

Compal Confidential

HBL50 Schematics Document

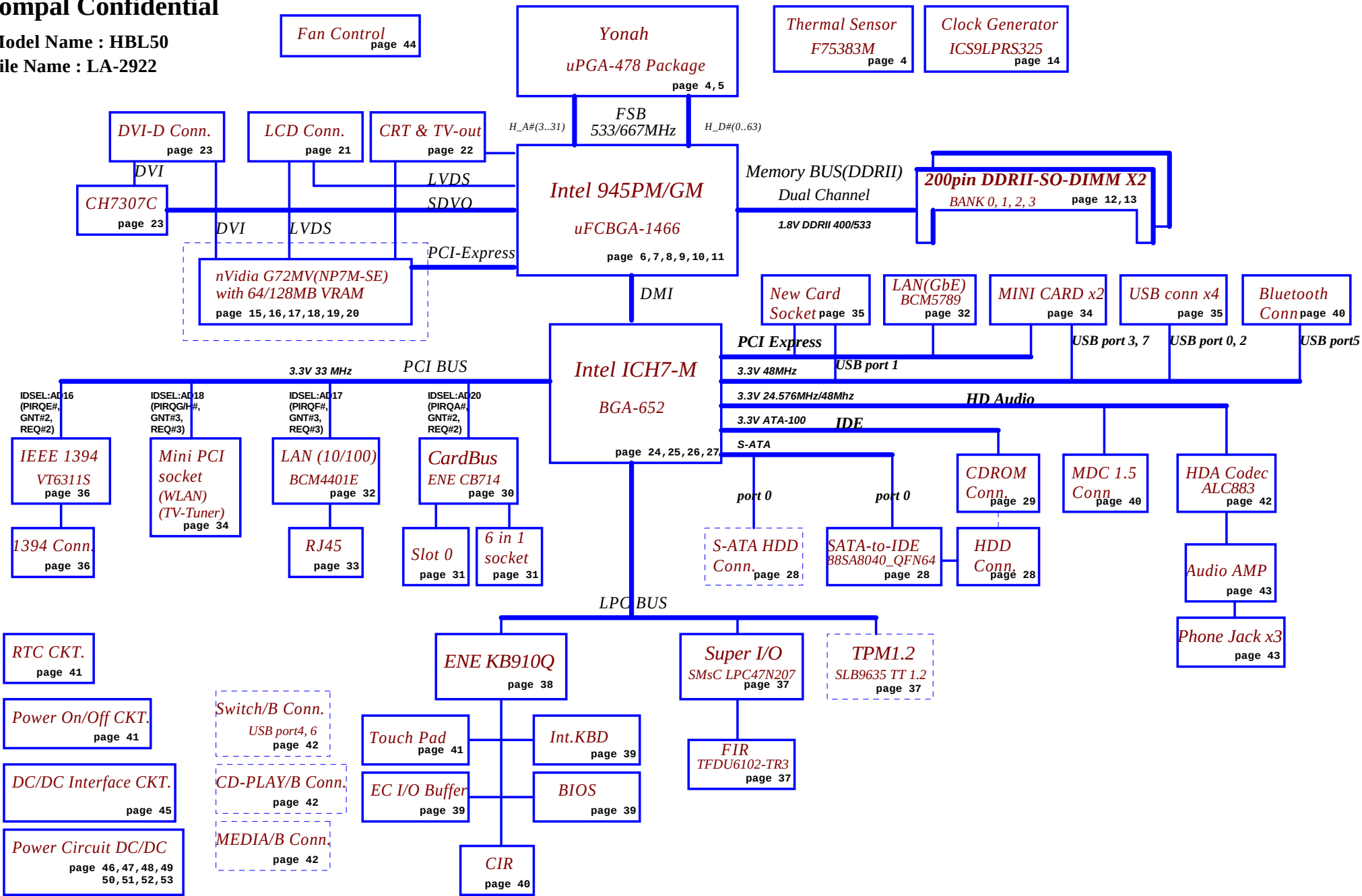
Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M
(With nVIDIA NB7M-SE)

2006-09-05
REV: 1.0

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Model Name : HBL50
File Name : LA-2922



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

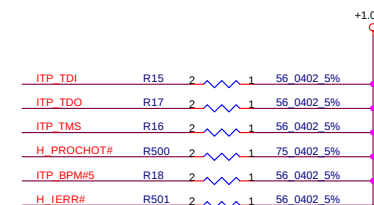
SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

G72MV	G72MV@
	G72MV64@
	G72MV128@
G72MZ	G72MZ@
G73	G73M128@

BTO Option Table

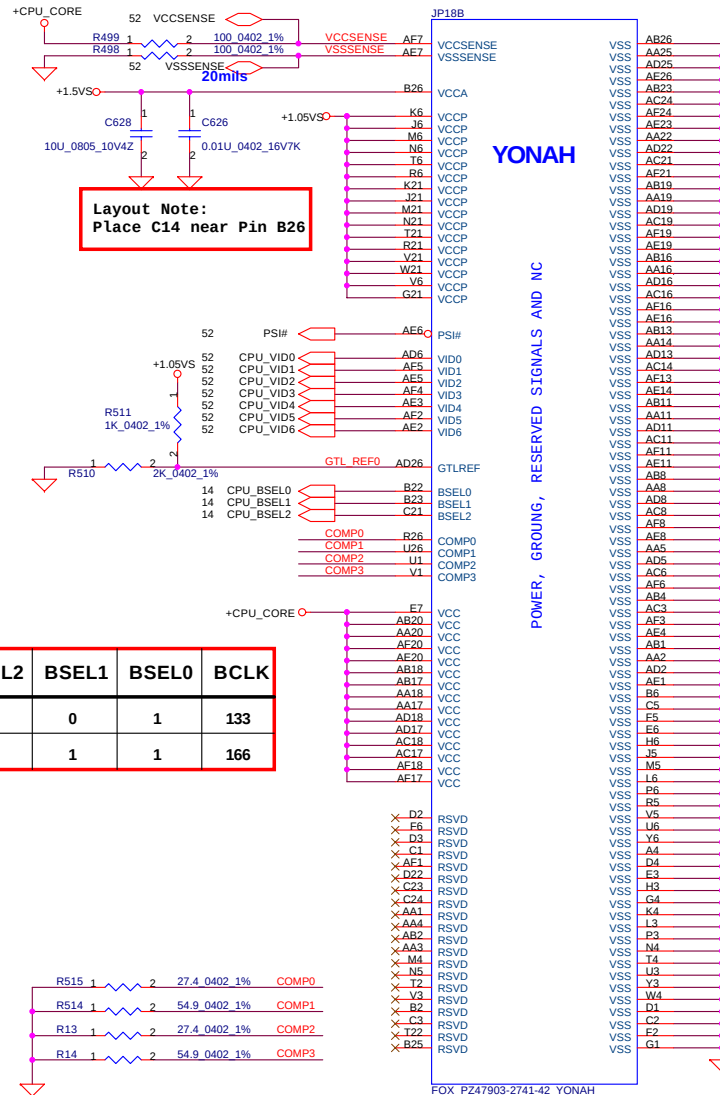
BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI_CARD1	MINI1@
MINI_CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
G72MV Only	G72@
G73 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@
DVI	DVI@
CardReader	4IN1@
New Card	EXP@

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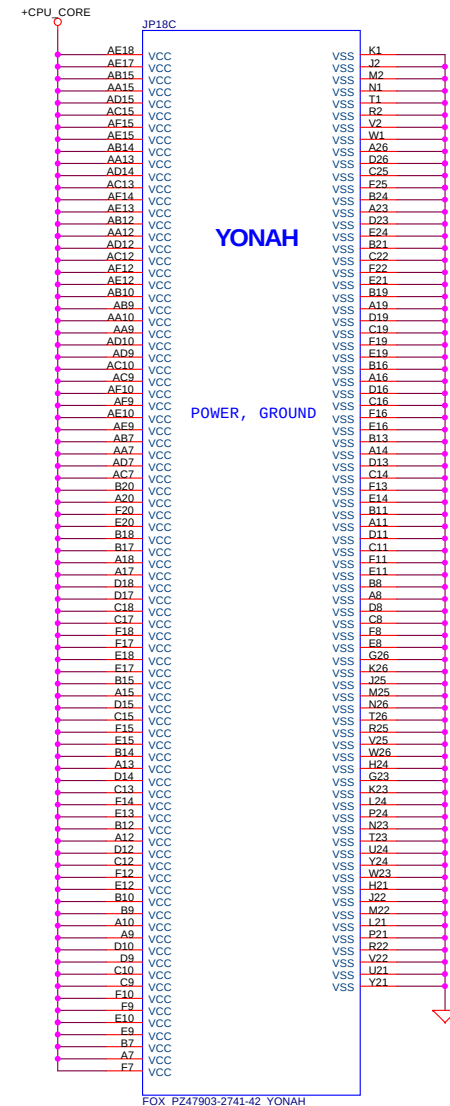
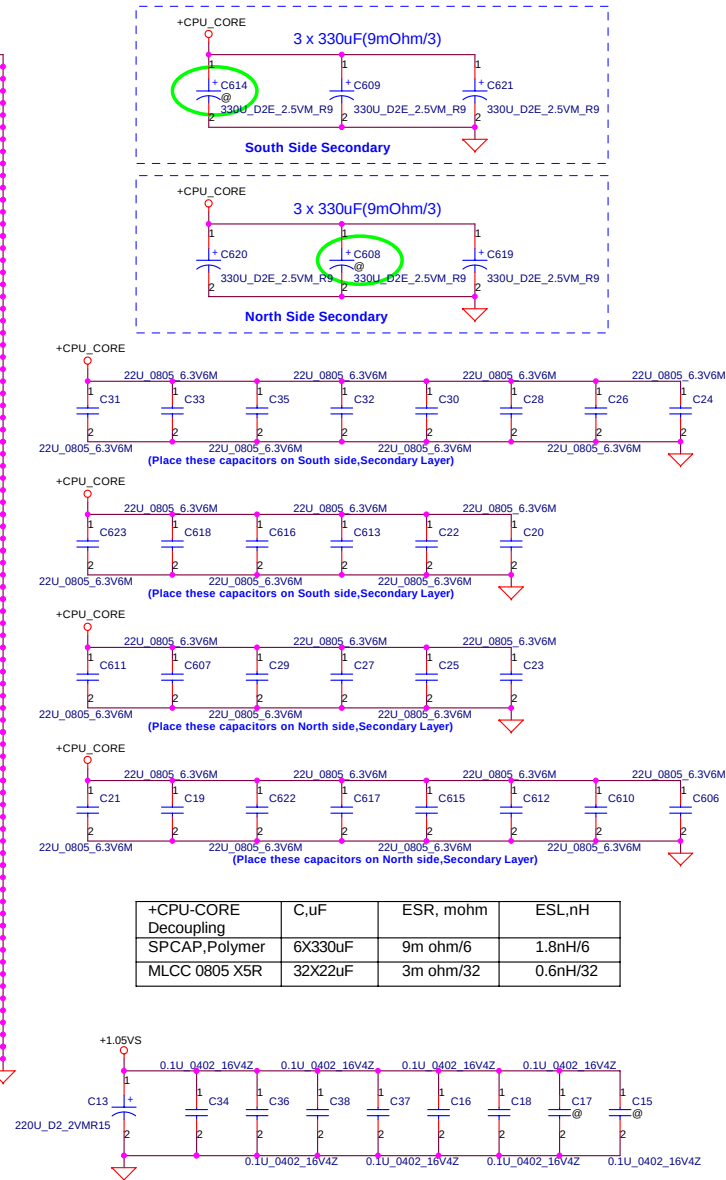
Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.40hms
with 50 mil spacing.
Place PU and PD within 1 inch of CPU.



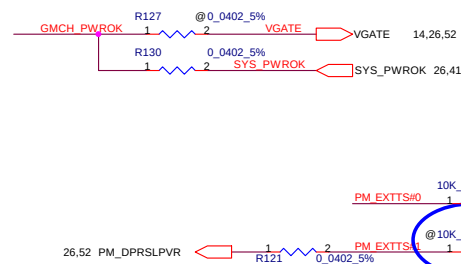
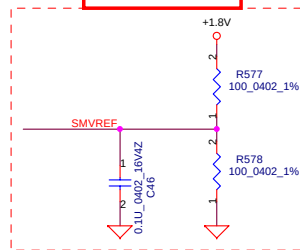
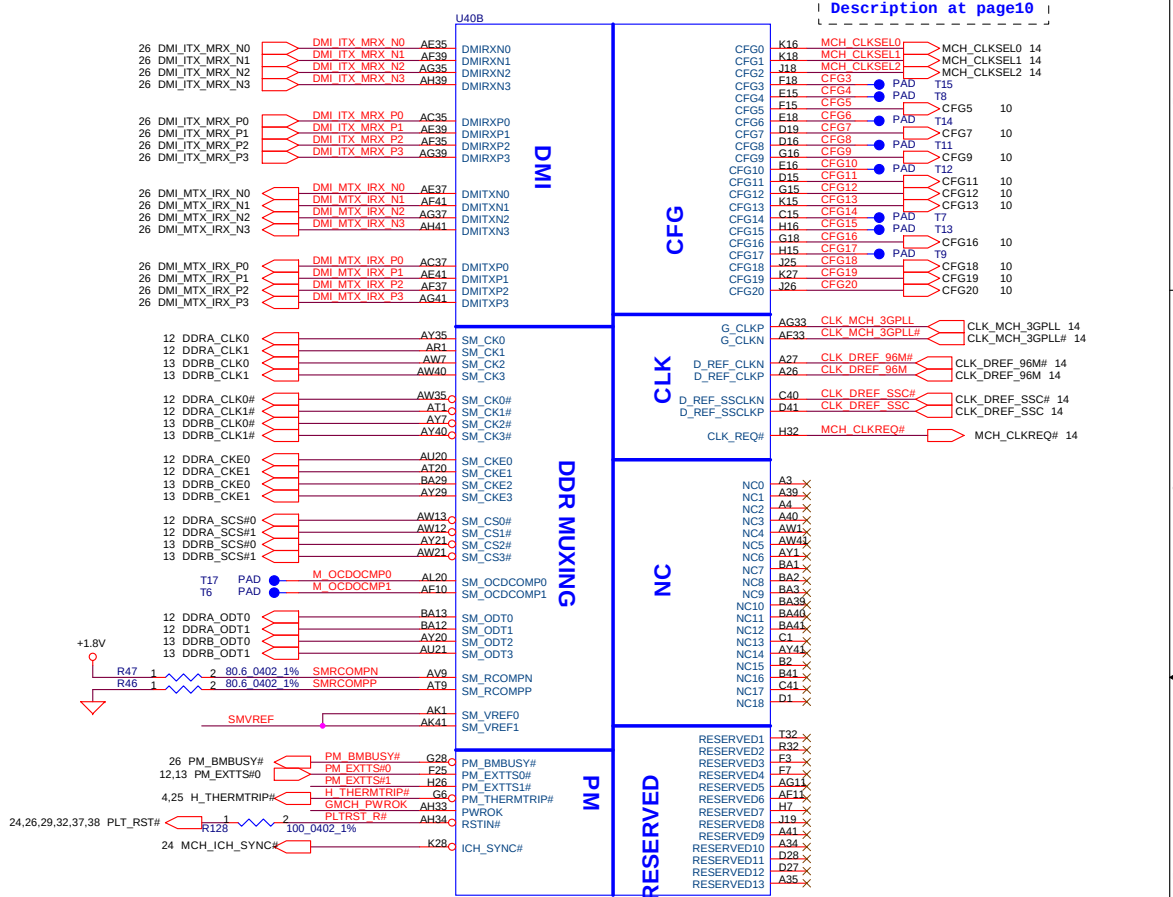
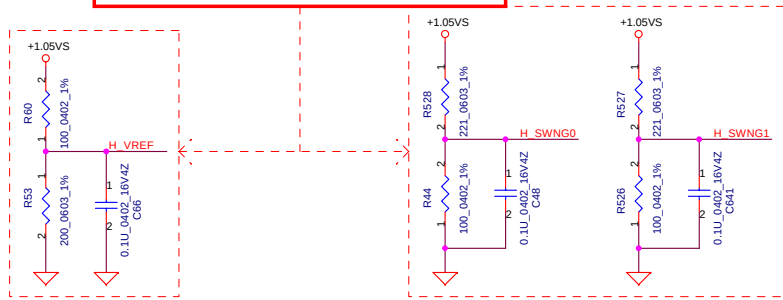
BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166

TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.40hms)
COMP1, COMP3 layout : Space 25mils (550hms)

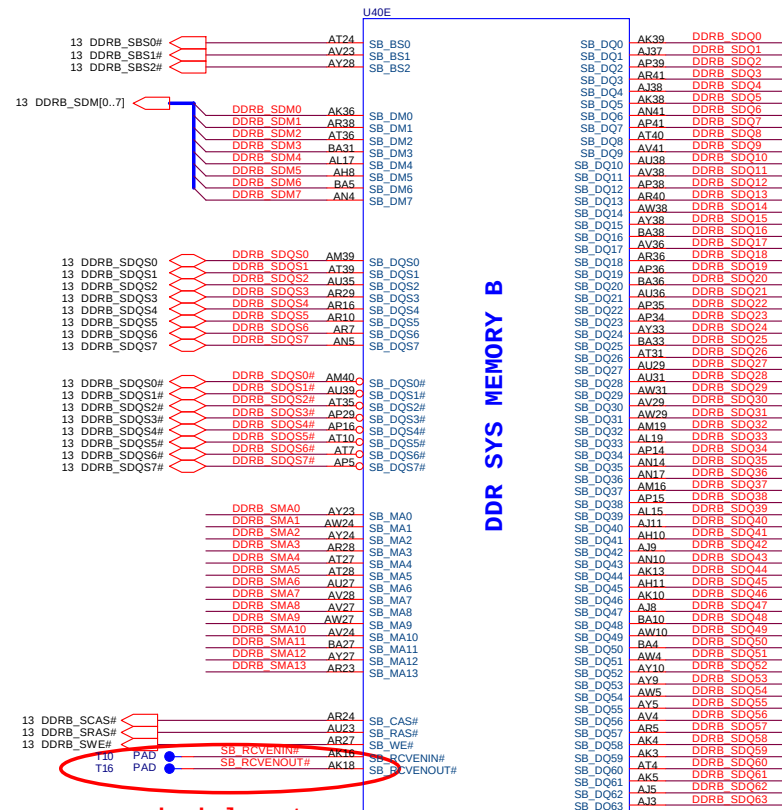


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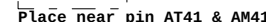


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CFG[3:17] have internal pull up
CFG[19:18] have internal pull down



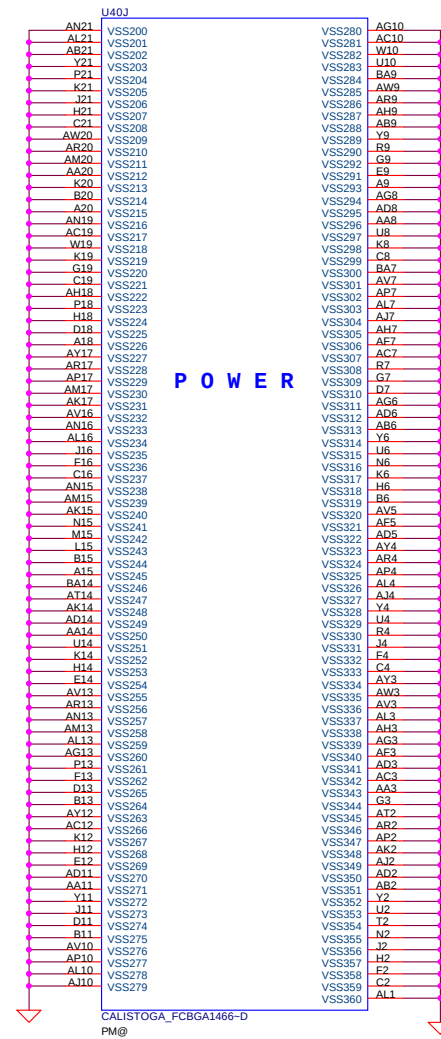
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Pin	Label	Value	Unit	Value	Unit	Value	Unit
6	CFG5	R58	1	2	@	2.2K	0.402 5%
6	CFG7	R81	1	2	@	2.2K	0.402 5%
6	CFG9	R67	1	2	@	2.2K	0.402 5%
6	CFG11	R57	1	2	@	2.2K	0.402 5%
6	CFG12	R59	1	2	@	2.2K	0.402 5%
6	CFG13	R69	1	2	@	2.2K	0.402 5%
6	CFG16	R68	1	2	@	2.2K	0.402 5%

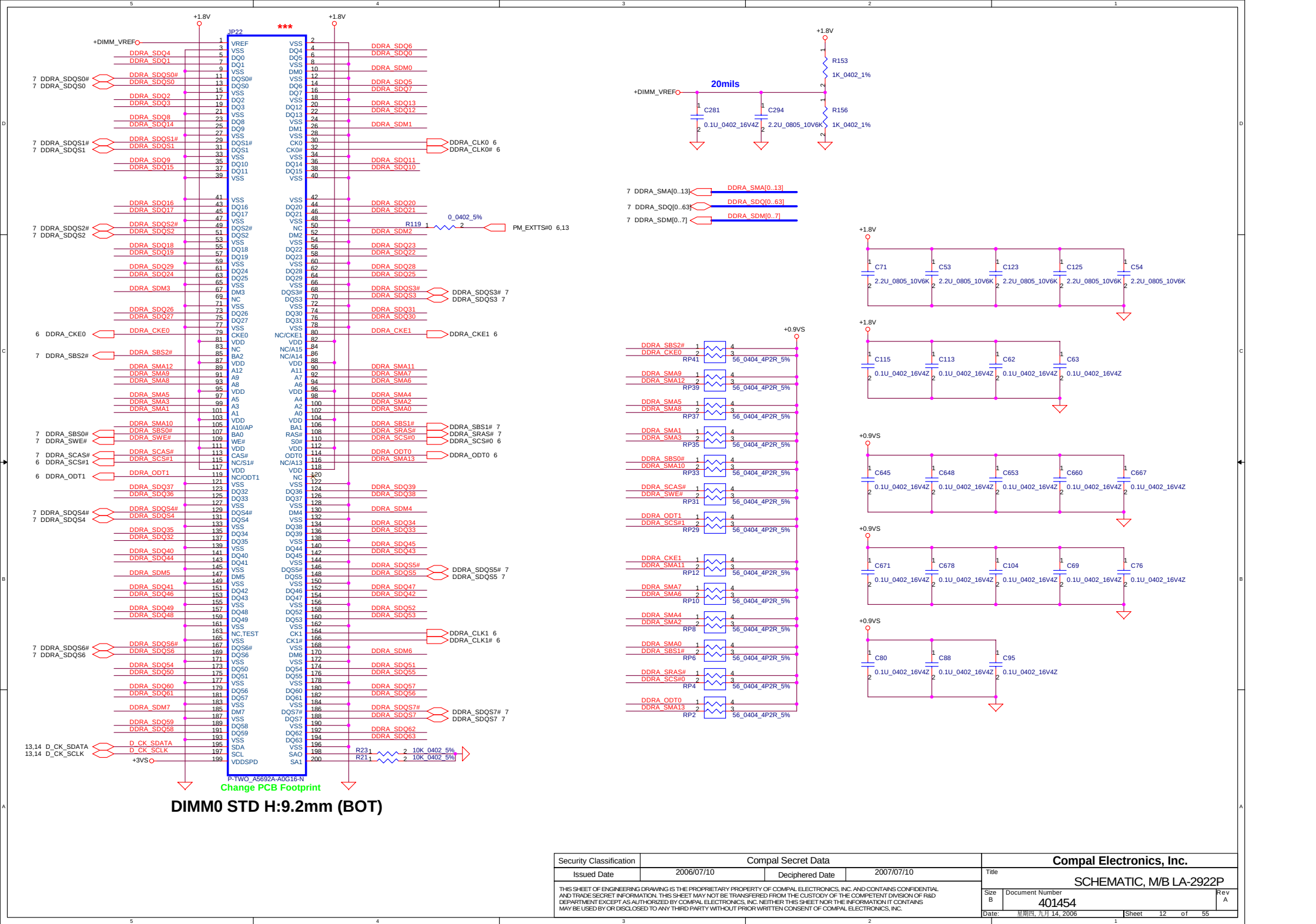
+3VS

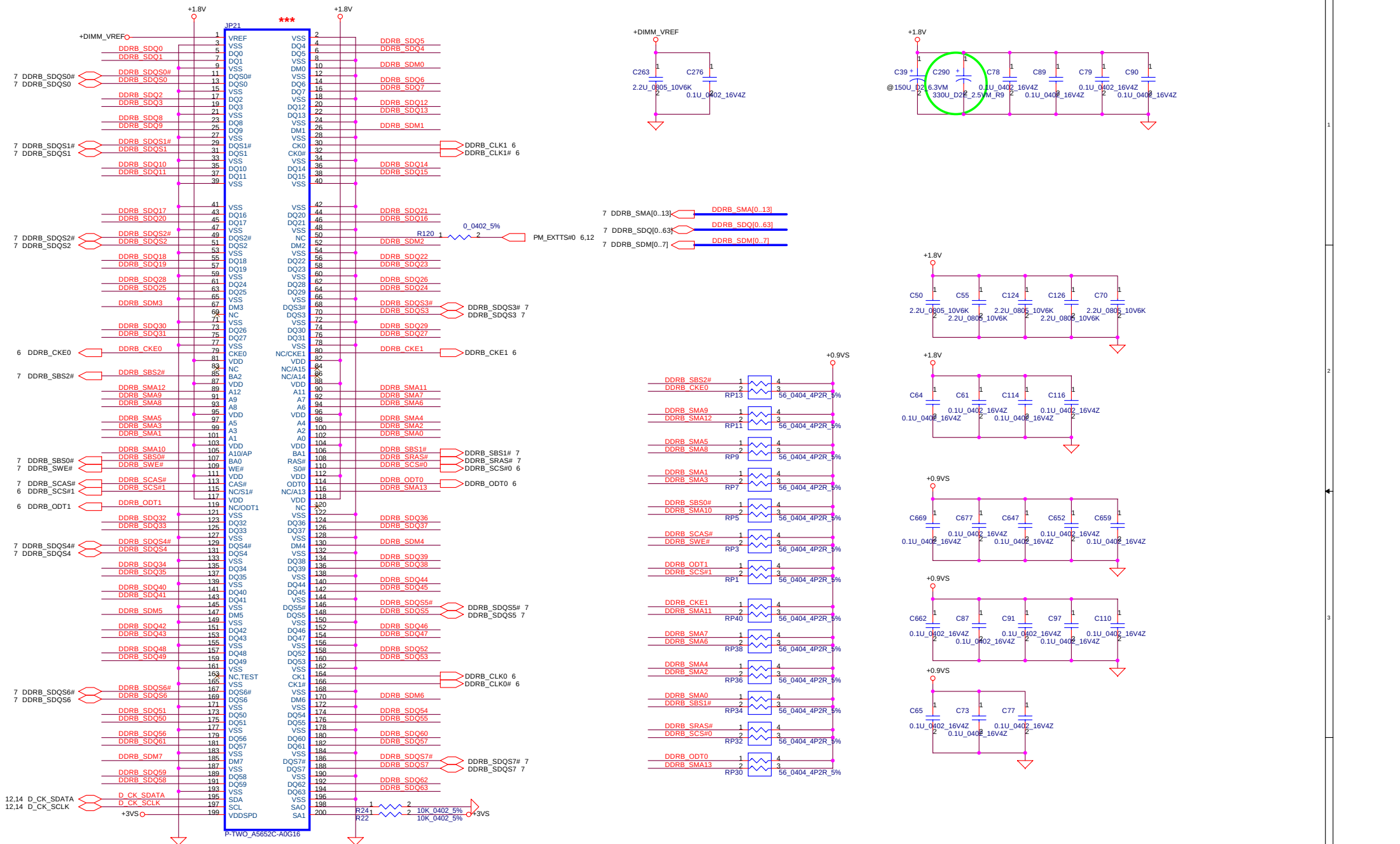
Pin	Label	Value	Unit	Value	Unit	Value	Unit
6	CFG18	R92	1	2	@	1K	0.402 5%
6	CFG19	R95	1	2	@	1K	0.402 5%
6	CFG20	R118	1	2	@	1K	0.402 5%

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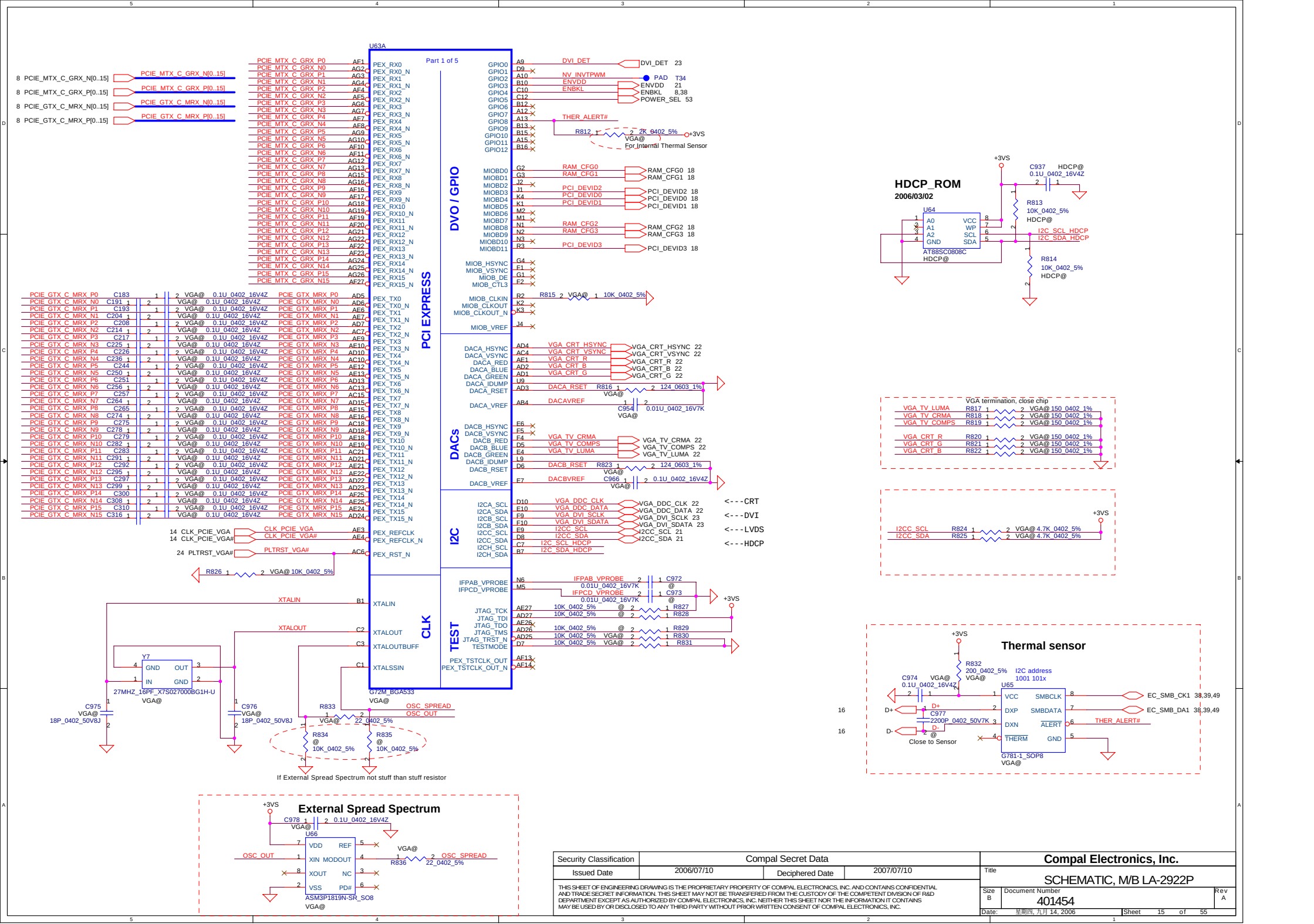
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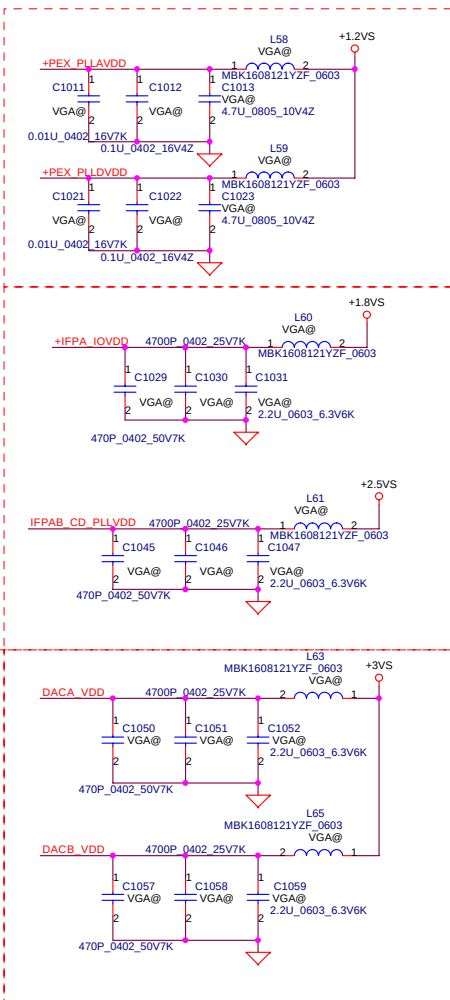
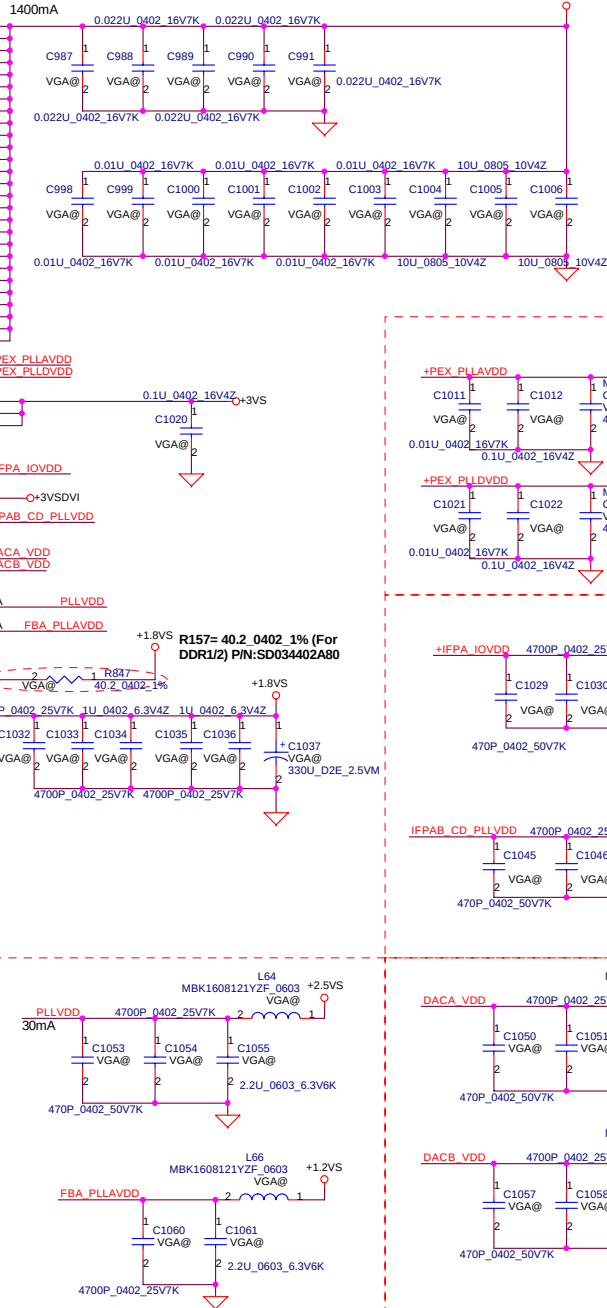
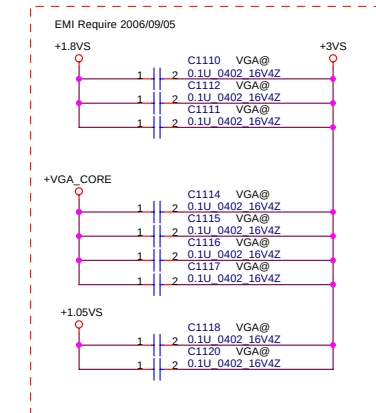
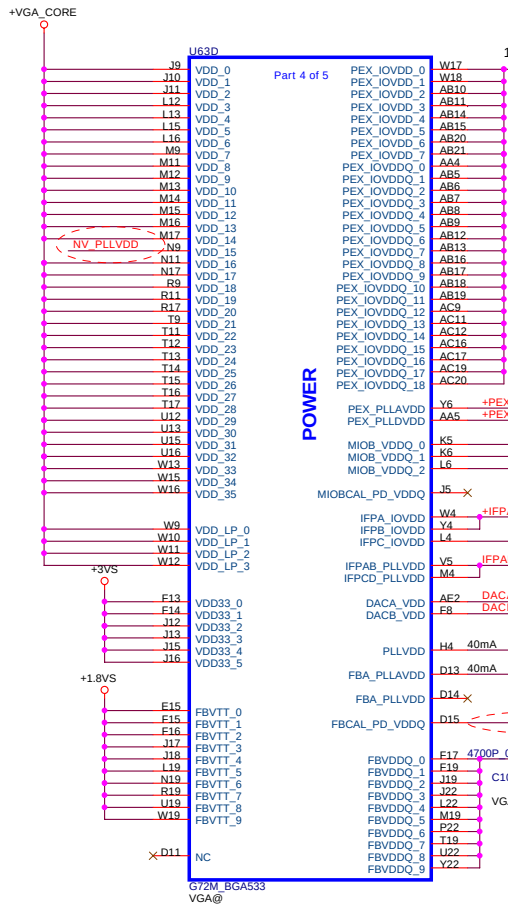
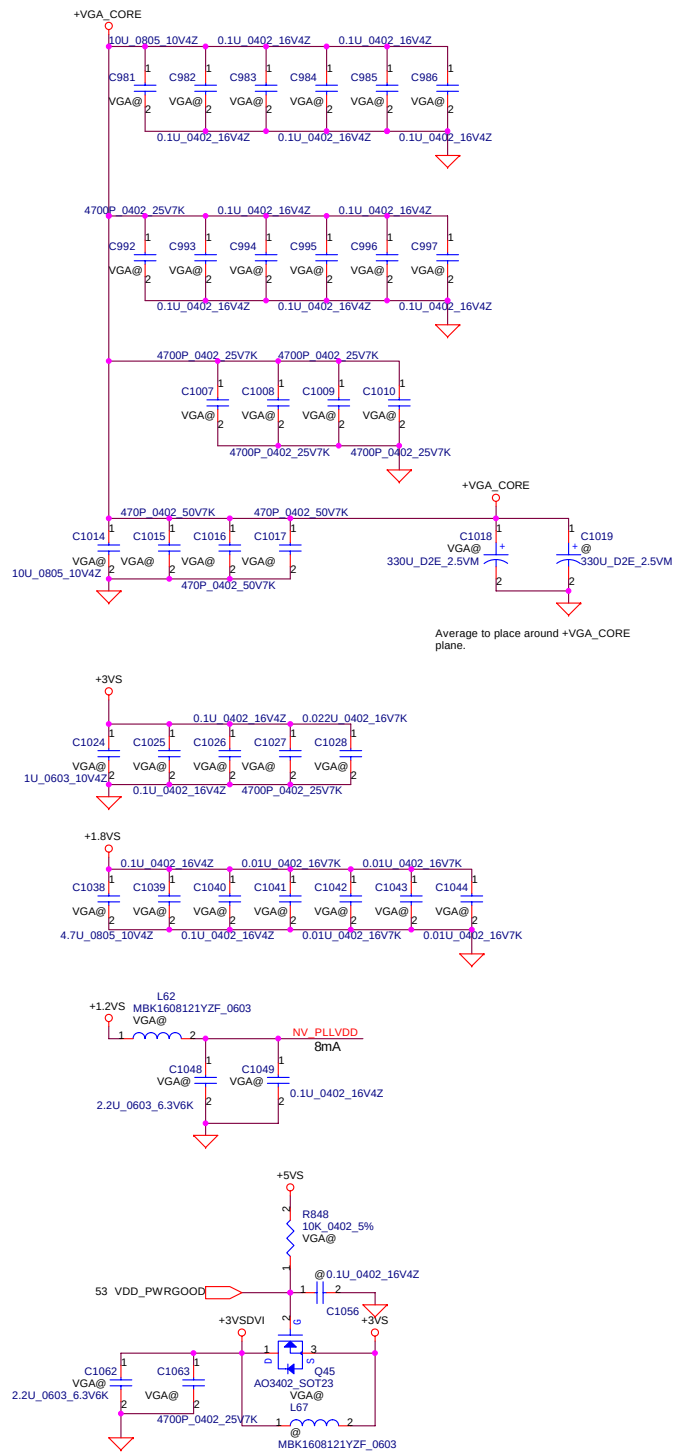
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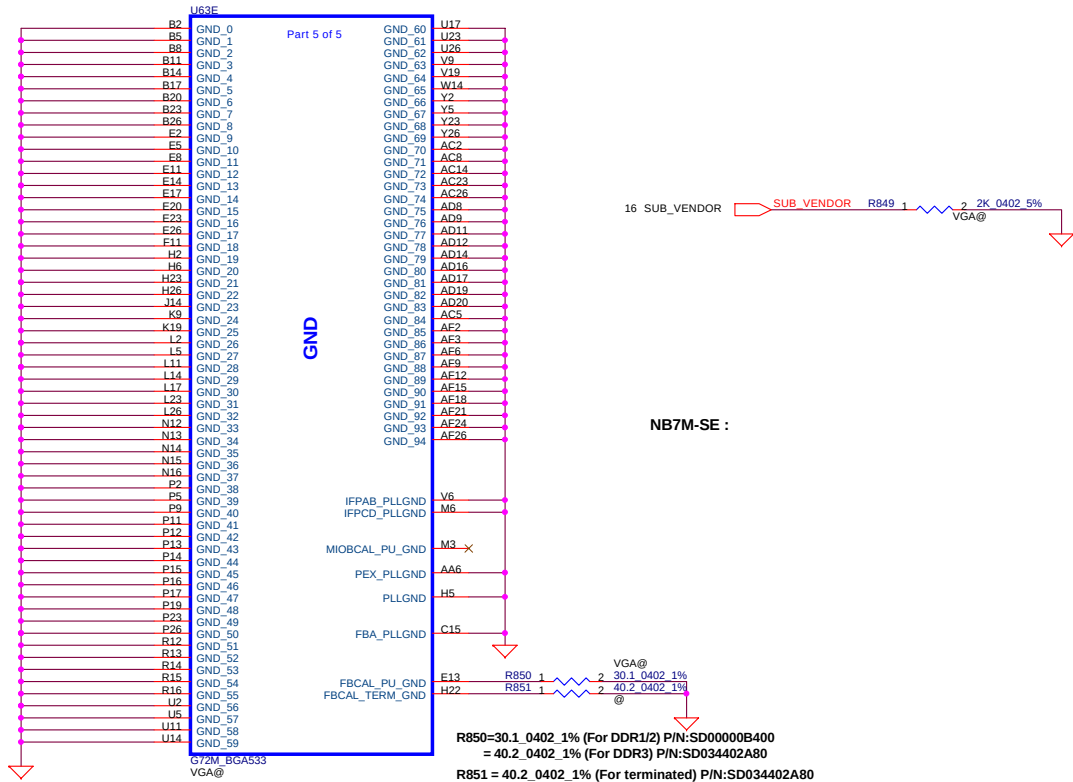


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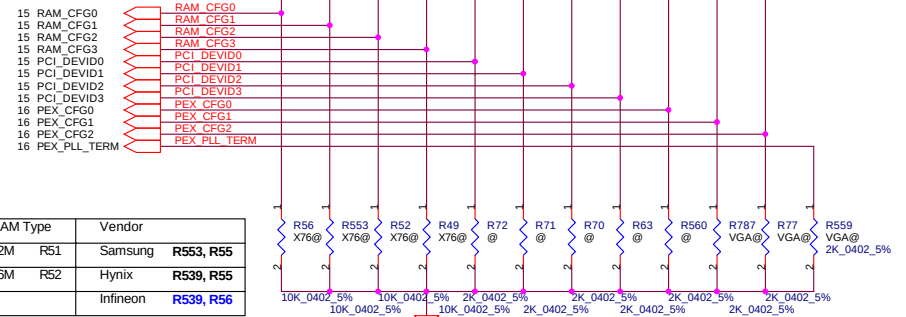




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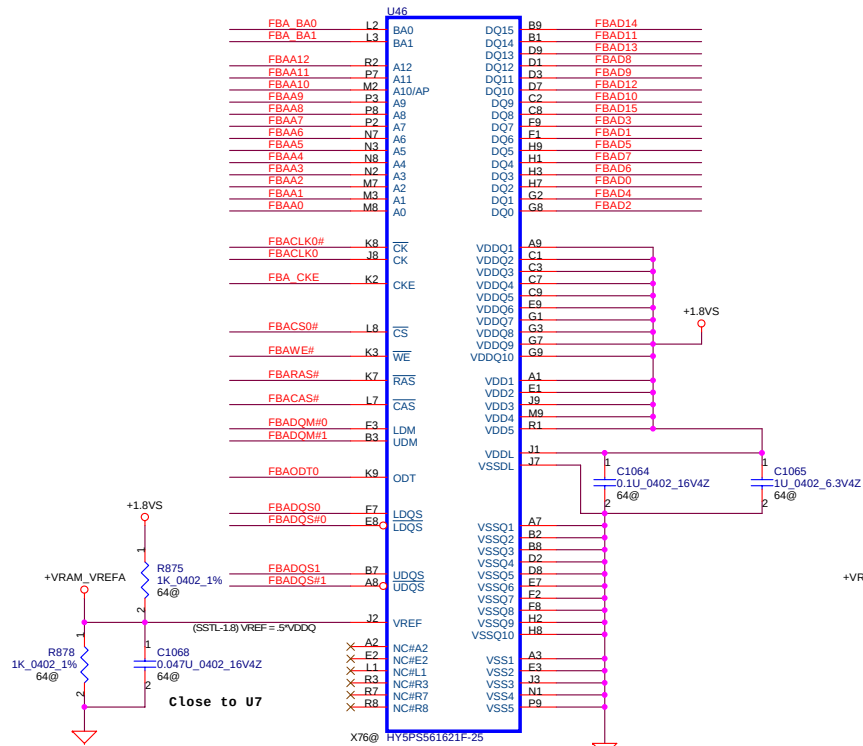
G73M		G72MV		
STRAPS	PIN	DESCRIPTION	Value	Value
SUB_VENDOR	MIOAD1	VB10S on card (pull high) VB10S with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9,8,6]	Recommended for G7x	001	
RAM_CFG[3:0]	MIOAD[5:2]	RAM_CFG[3] (Bandwidth 0=Full, 1=Half)		
		RAM_CFG[2] (0=16M or 1=32M)		
		RAM_CFG[1:0] (Manufacture) (01=Sam, 10=Inf, 11=Hyn)		
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxxx8 G72M-0x01D8	1000	
		G72MV-0x01D7 TBD/TBD	0111	



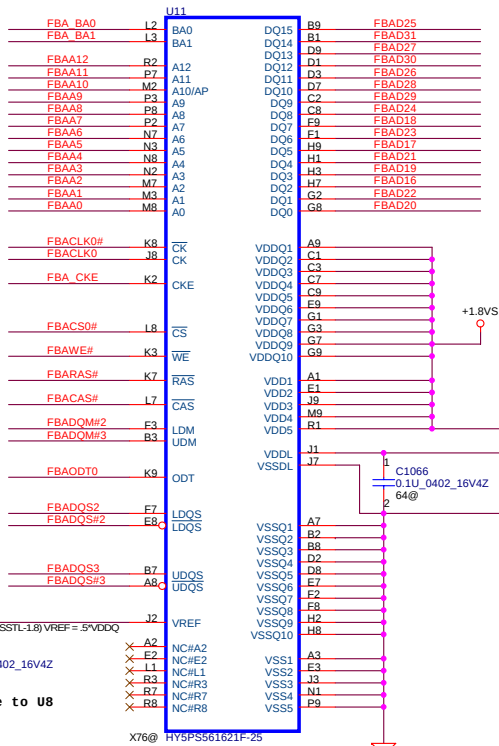
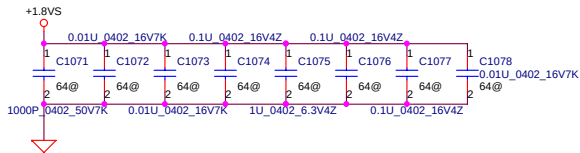
Bandwidth	RAM Type	Vendor
FULL R49	32M R51	Samsung R553, R55
HALF R48	16M R52	Hynix R539, R55
		Infineon R539, R56

Package		
(10*12.5)	Infineon GDDR2(400): SA00000S800 (HYB18T256161AF-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
(11*13)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
(8*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)

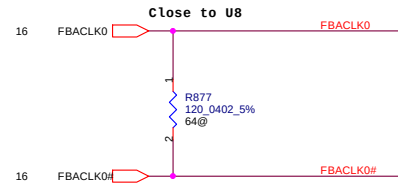
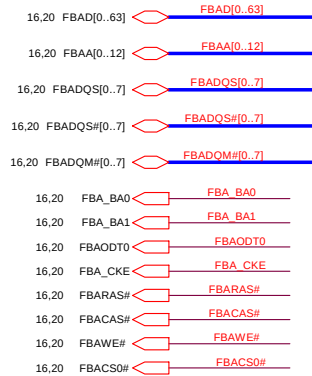
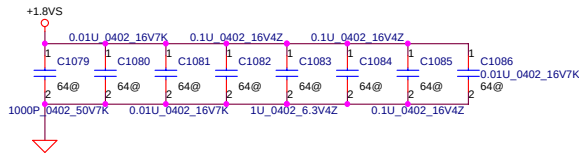
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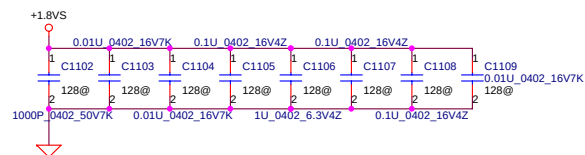
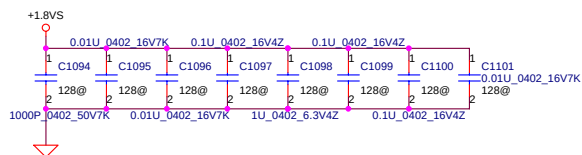
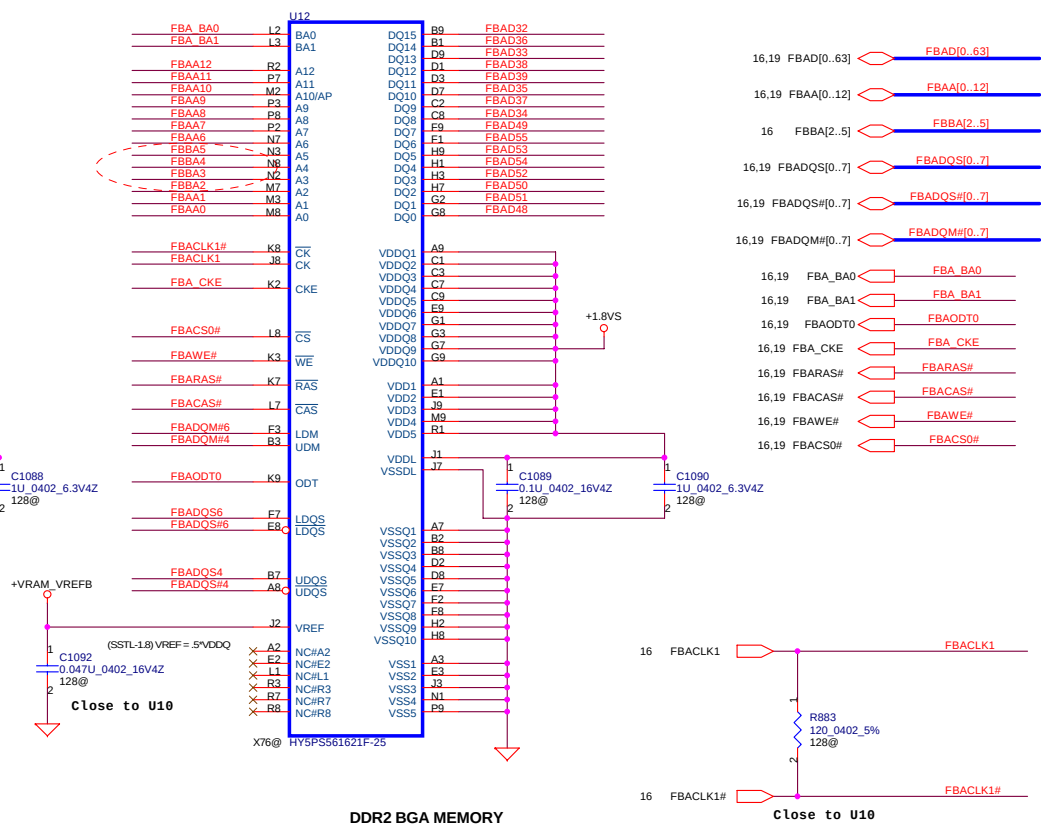


DDR2 BGA MEMORY



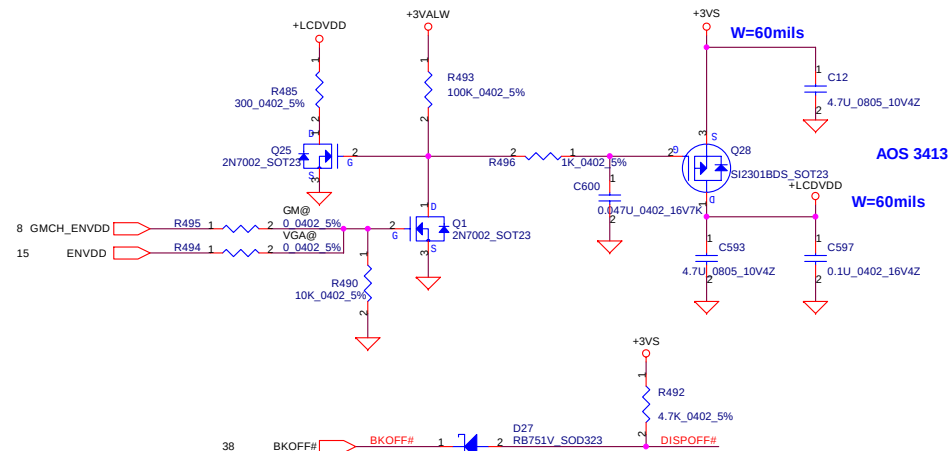
DDR2 BGA MEMORY



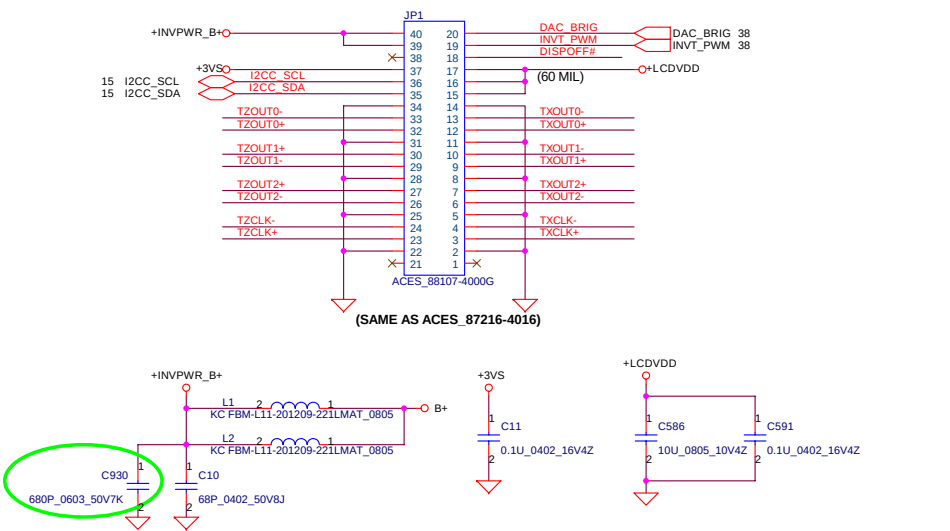


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				SCHEMATIC, M/B LA-2922P	
				Size Document Number CustId 401454	
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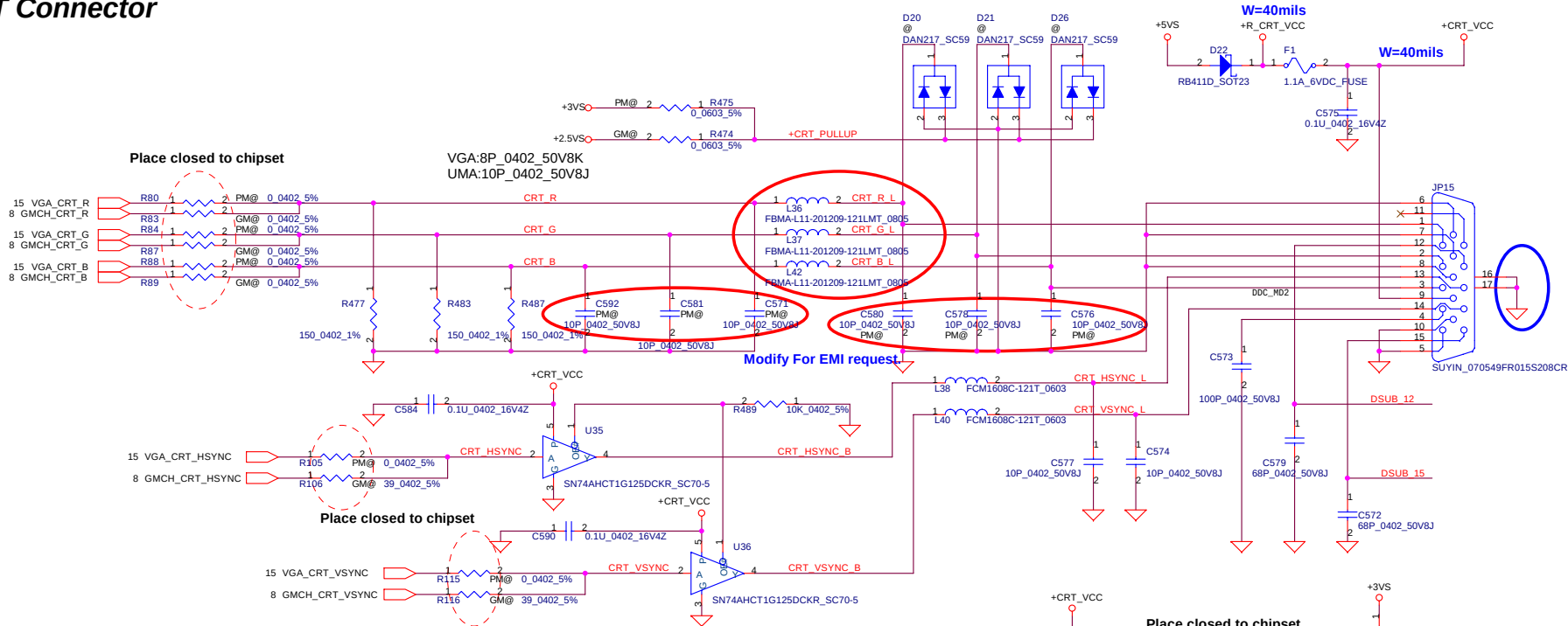
LCD POWER CIRCUIT



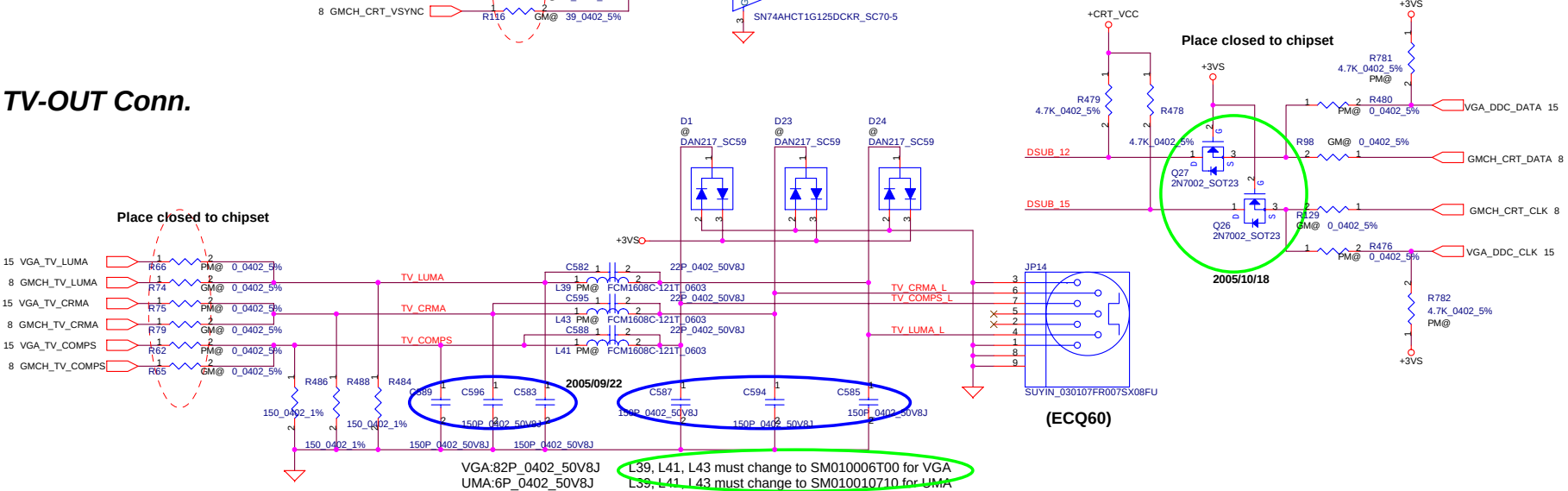
LCD/PANEL BD. Conn.



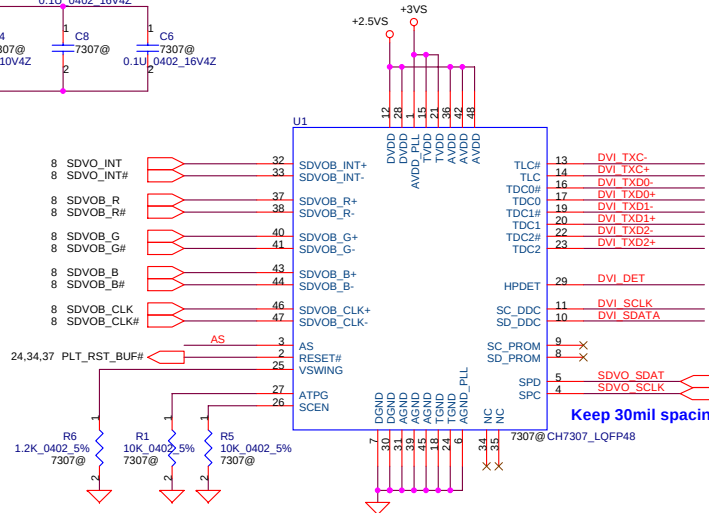
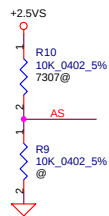
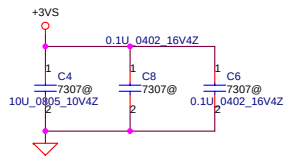
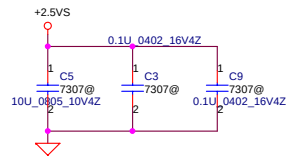
CRT Connector



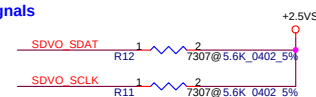
TV-OUT Conn.



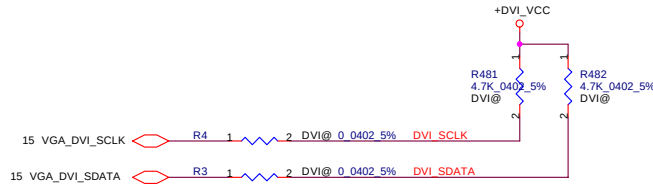
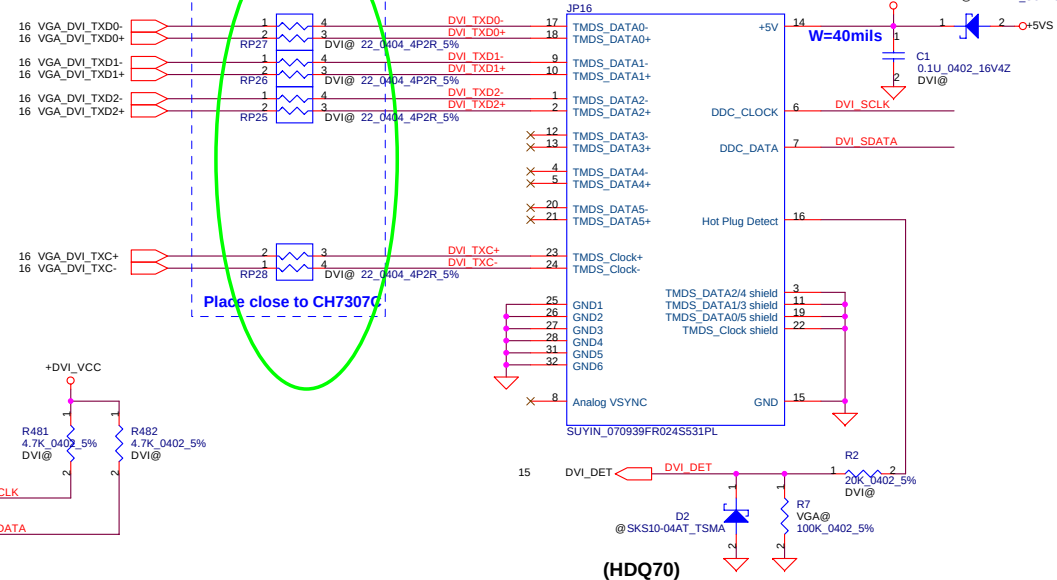
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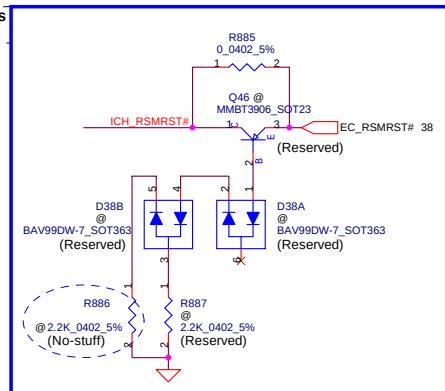
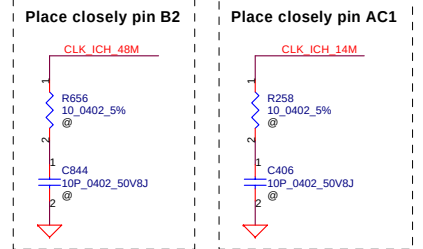
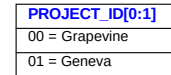
BOM structure	DVI from SDVO	DVI from Discrete VGA
7307@	Stuff	No_Stuff
VGA@	No_Stuff	Stuff
@	No_Stuff	No_Stuff



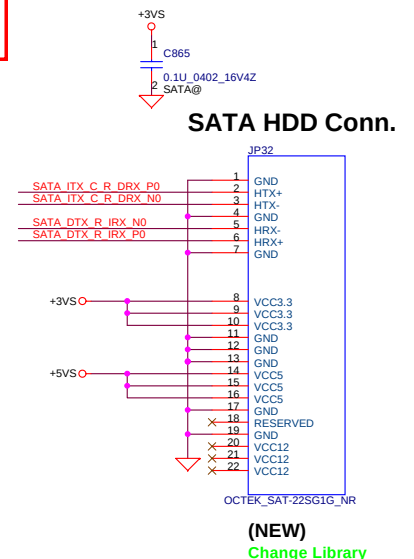
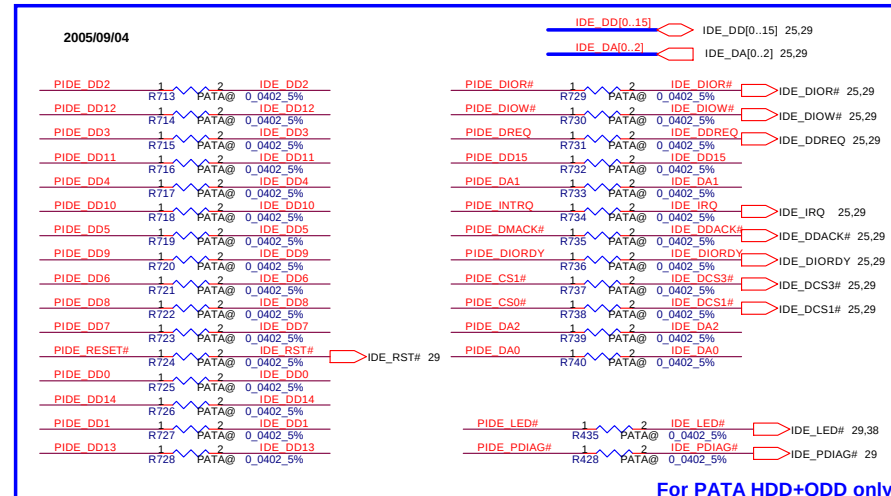
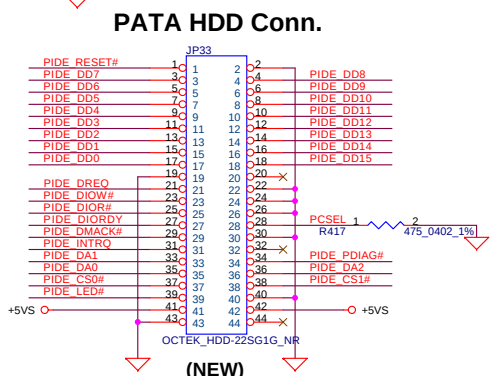
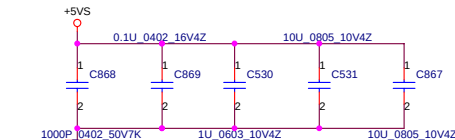
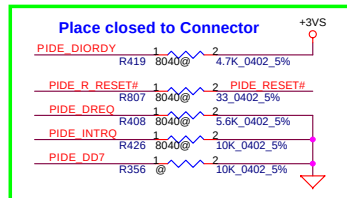
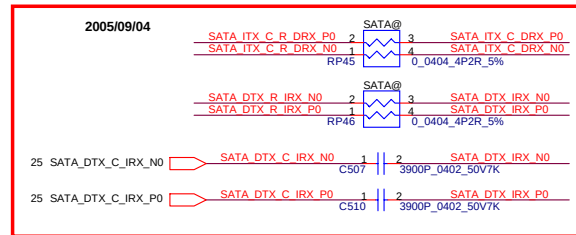
DVI-D Connector



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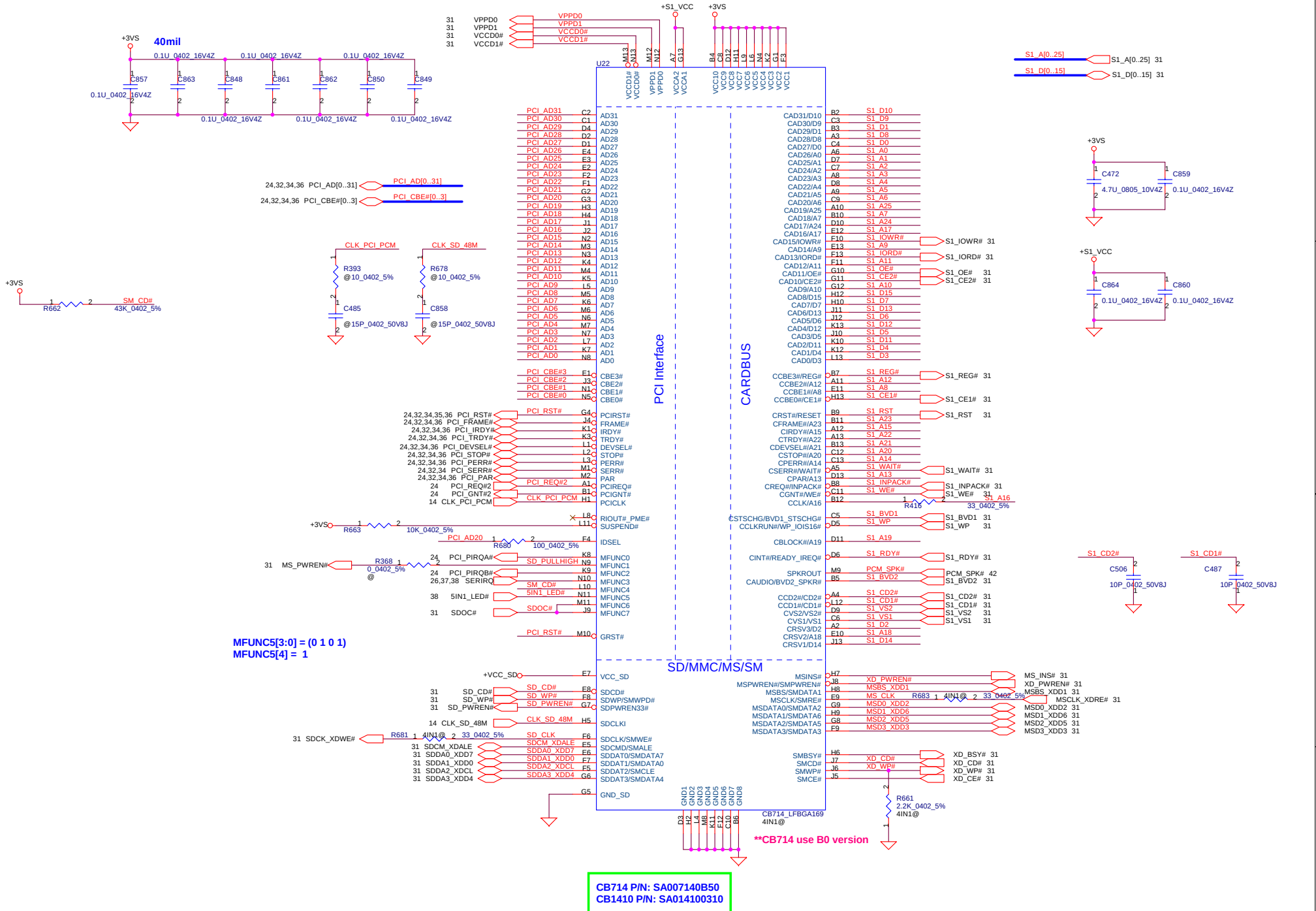
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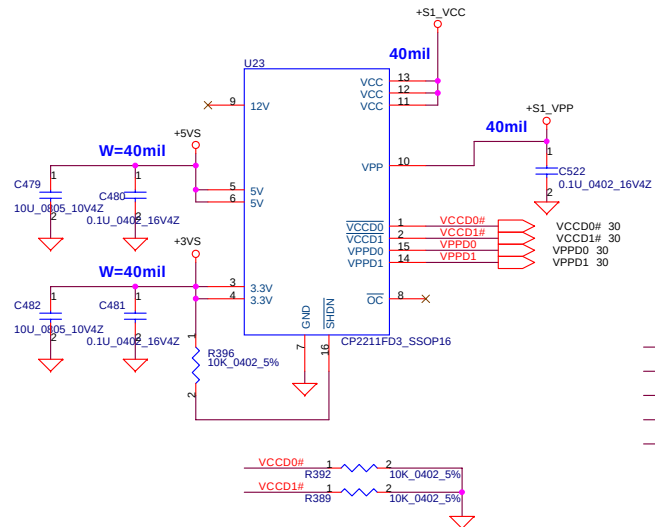


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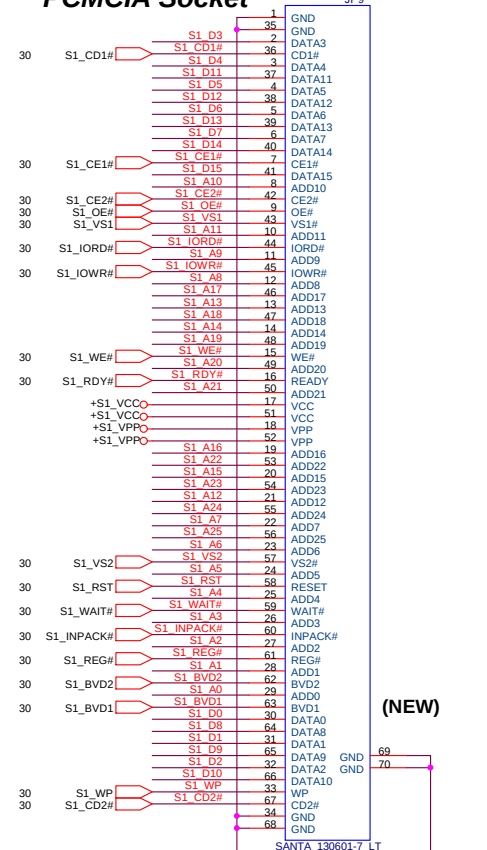
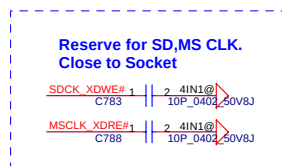
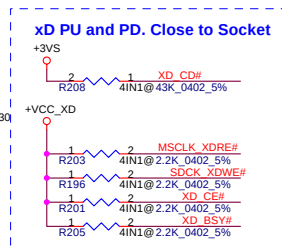
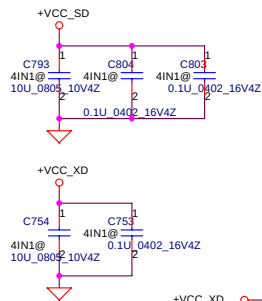
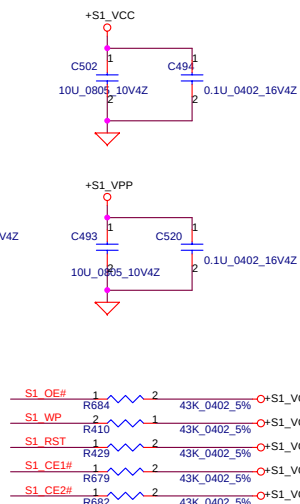
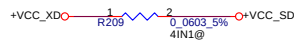
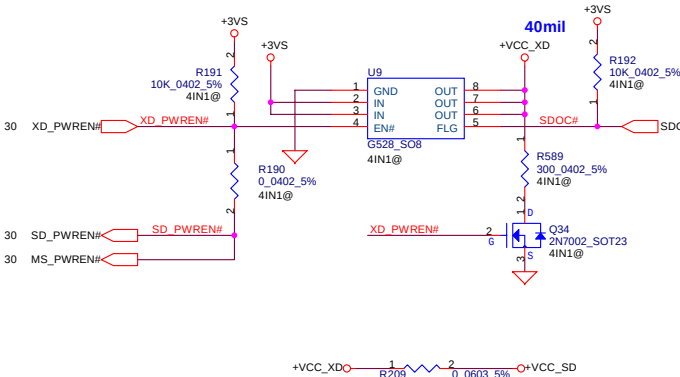


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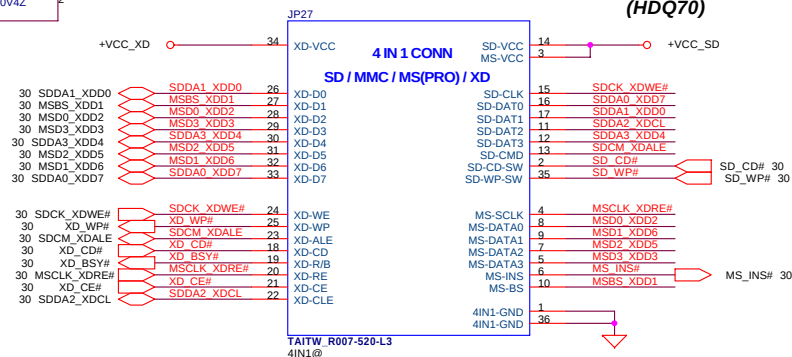
PCMCIA Power Control



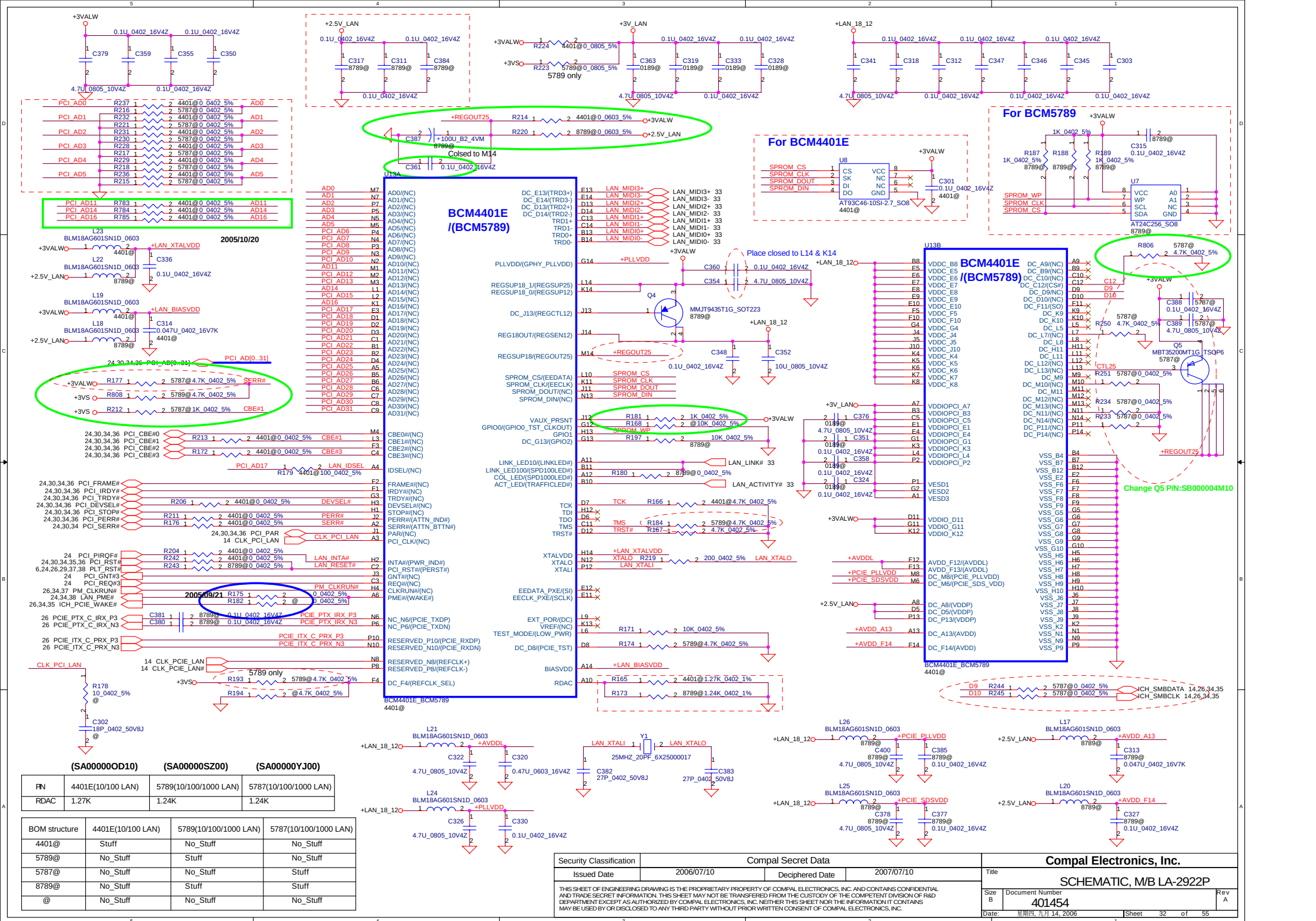
SD/MS Power Control
XD Power Control



4 IN 1 Socket
(HDQ70)



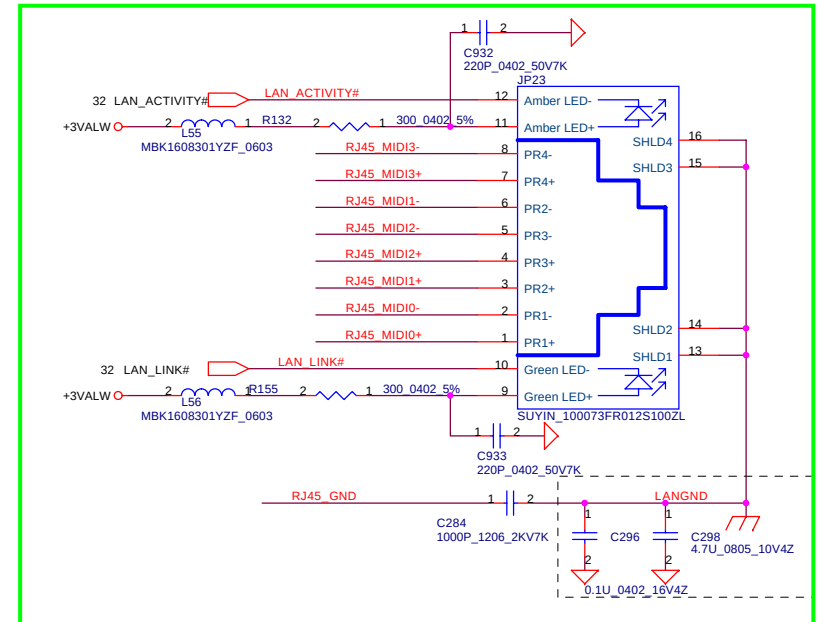
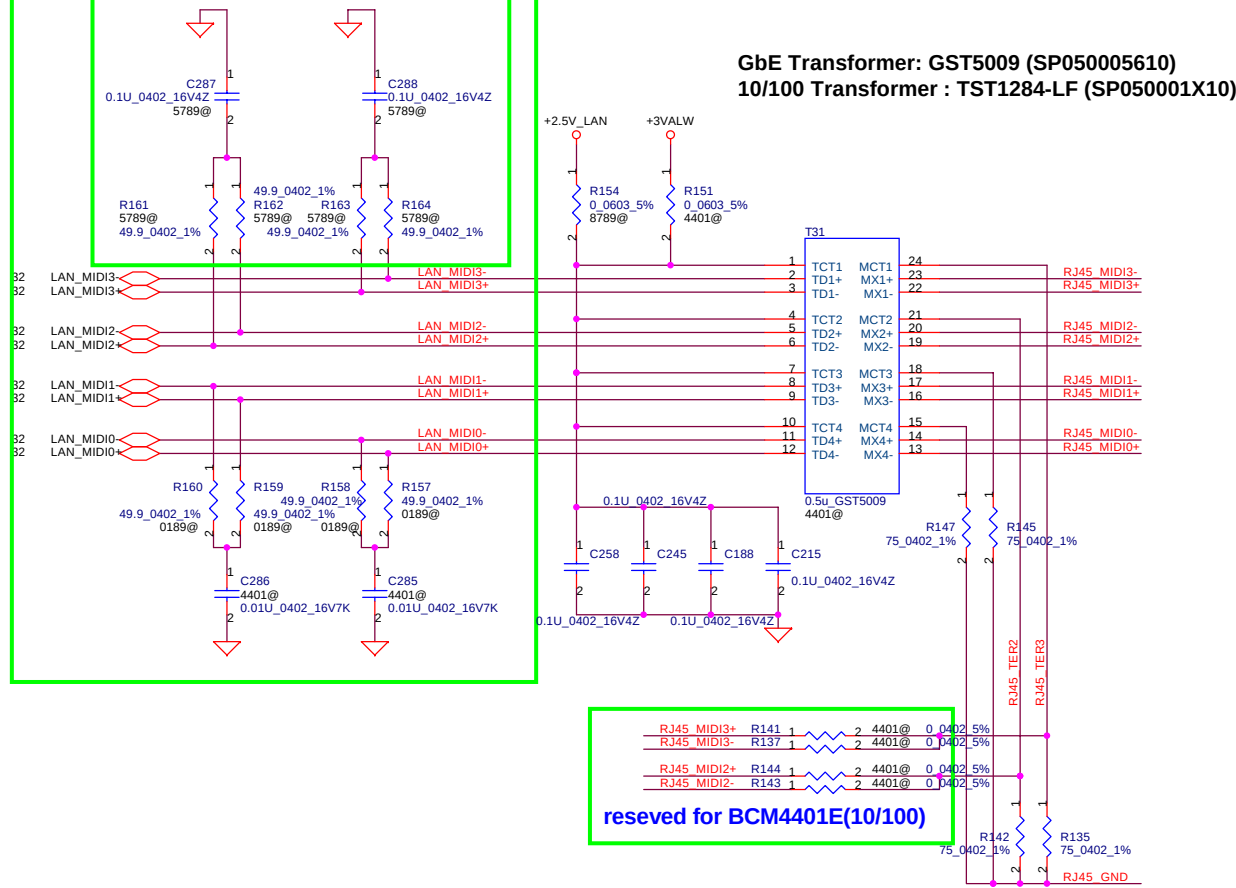
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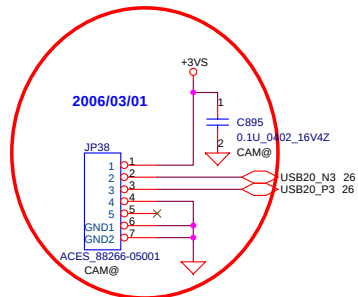
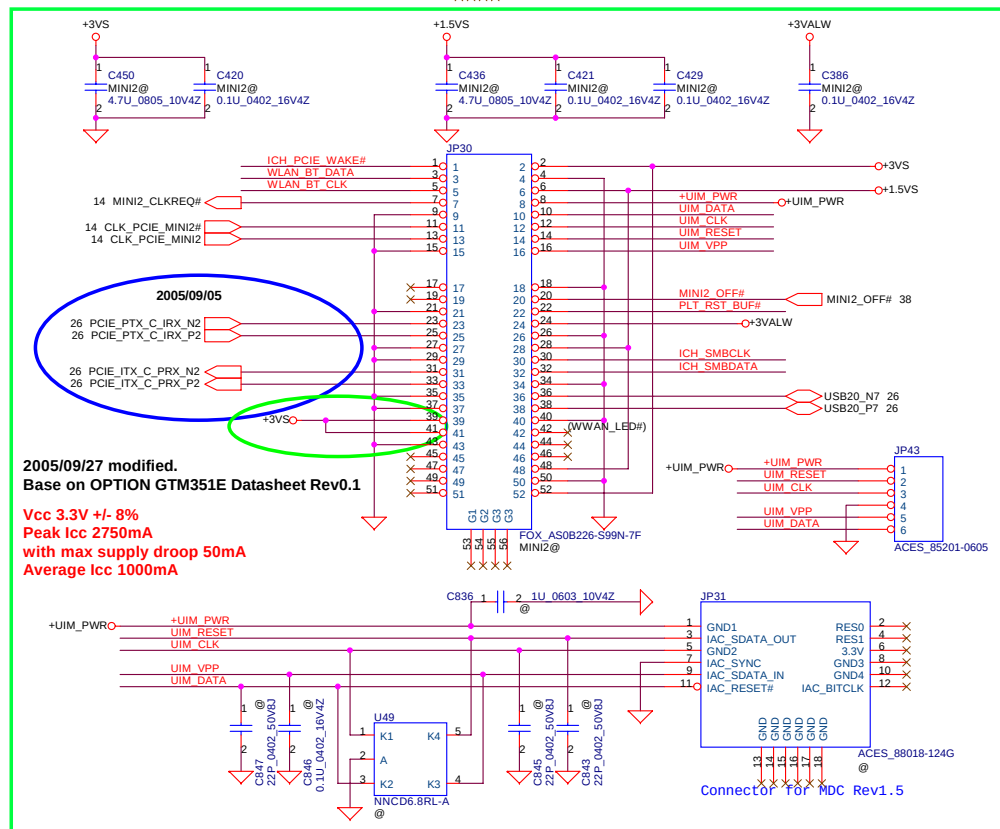
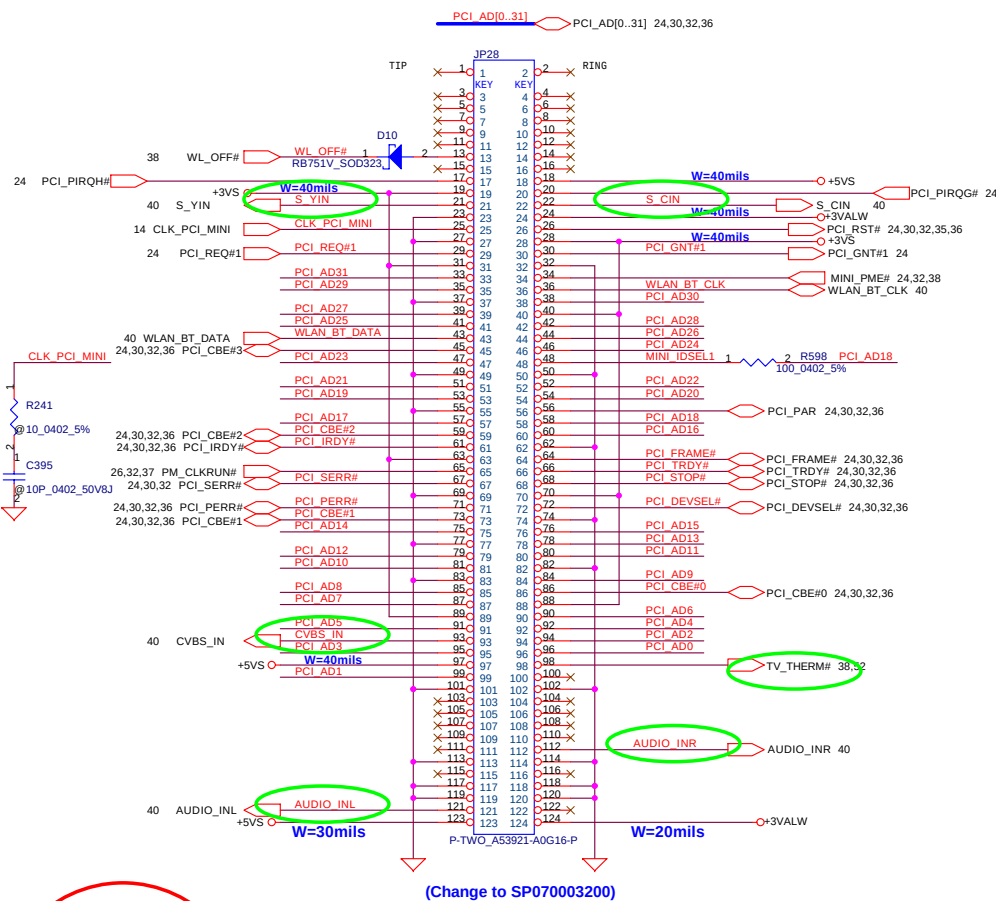
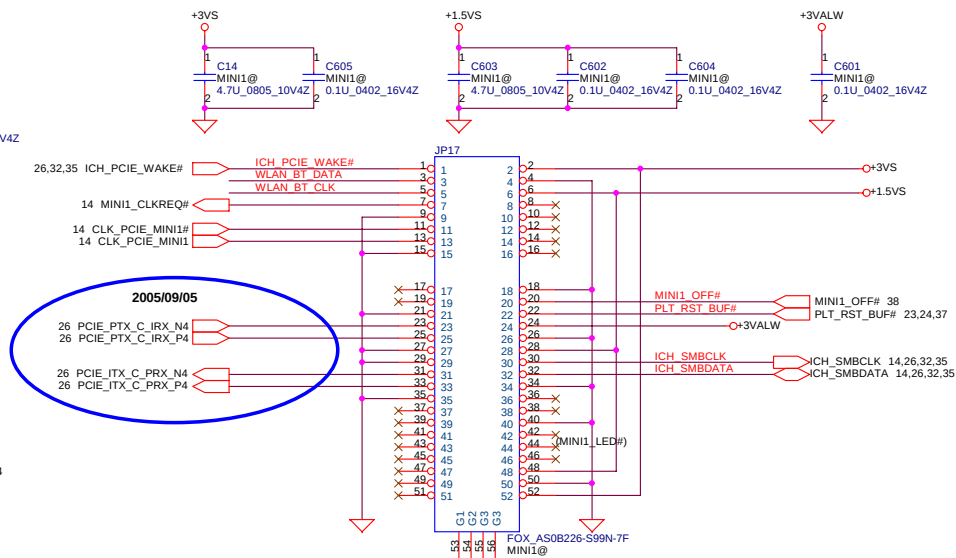
LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

unpop when use BCM4401E(10/100)

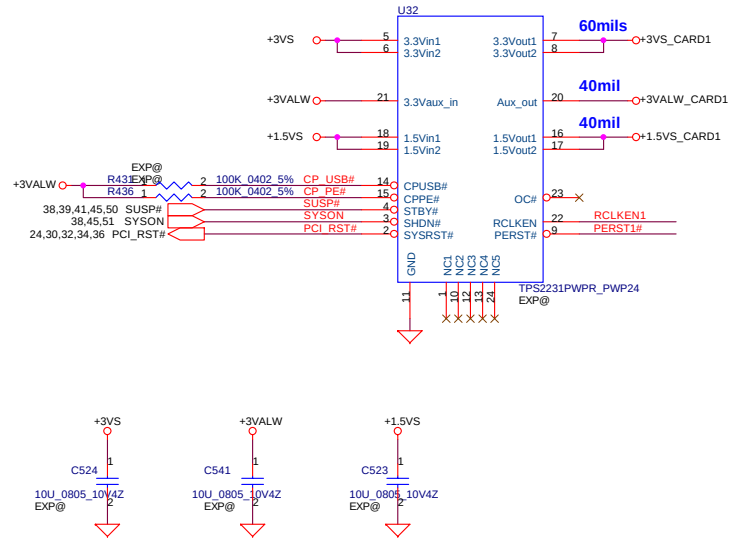


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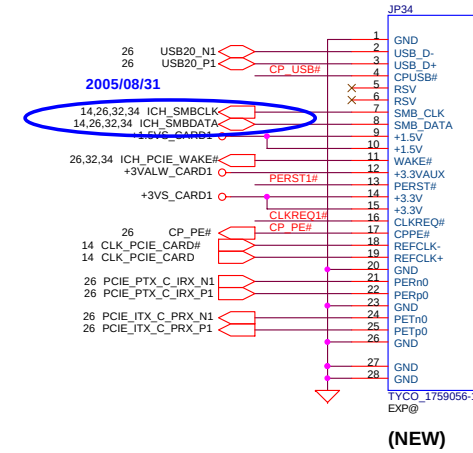


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

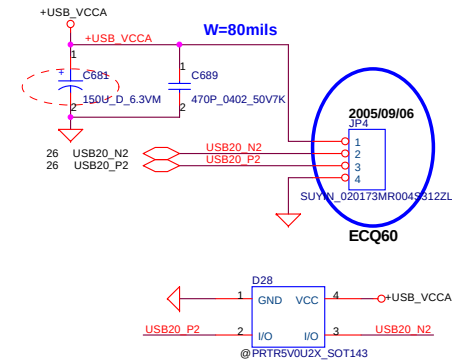
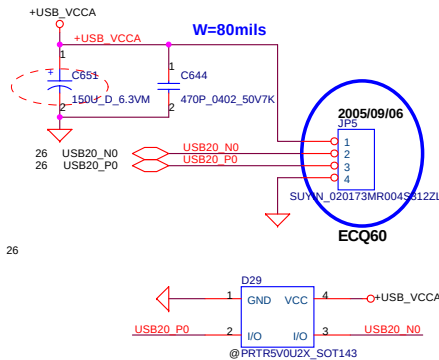
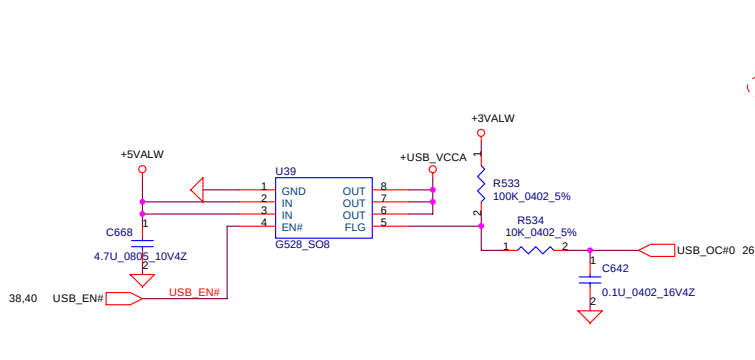
New Card Power Switch



New Card Socket (Left)



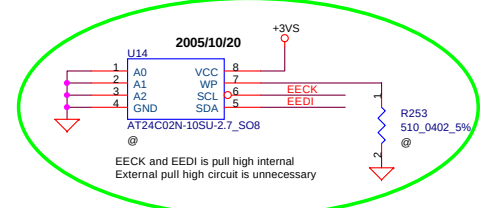
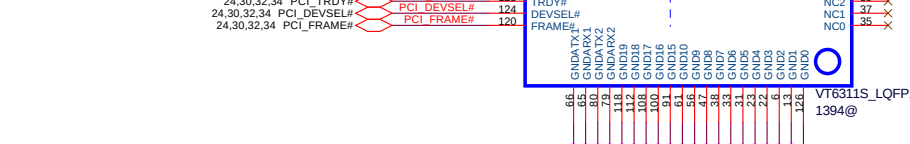
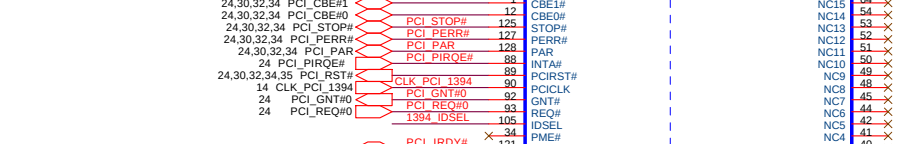
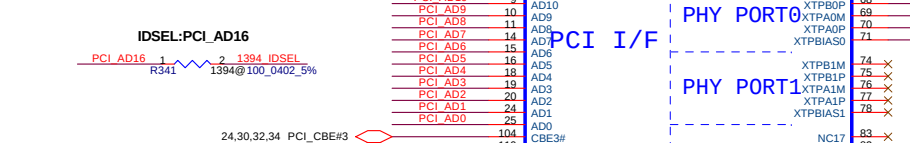
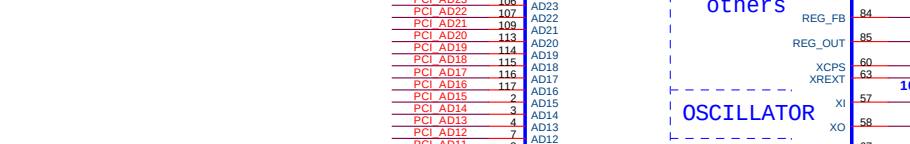
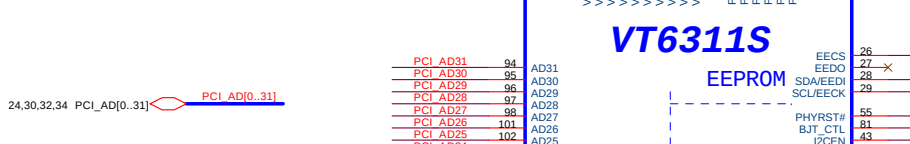
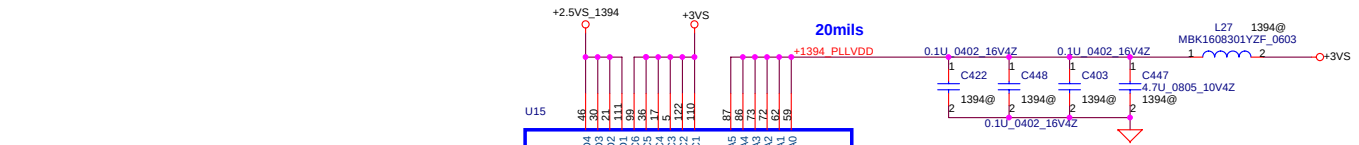
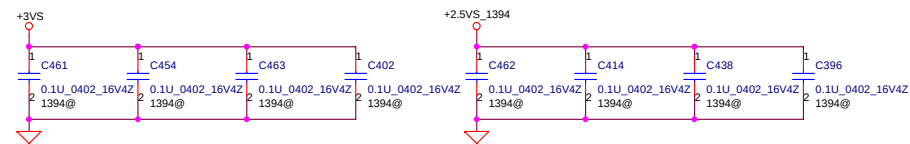
USB CONN. 1 & 2



SUYIN_020173MR004G533ZR_4P

SUYIN_020173MR004G533ZR_4P

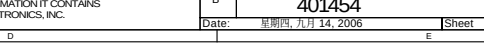
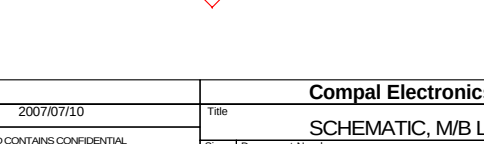
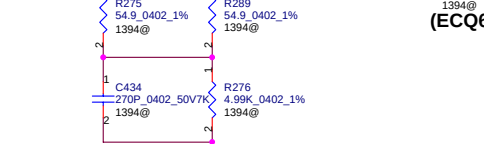
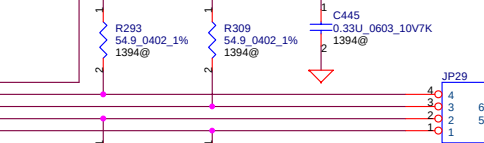
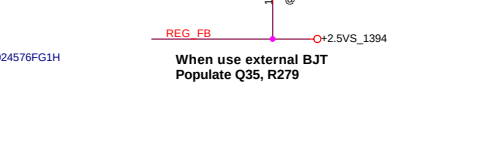
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When use external EEPROM
Populate U14, R246, R253
Un-populate R261



When use external BJT
Populate Q35, R279



VT6311S

EEPROM

others

OSCILLATOR

PHY PORT0

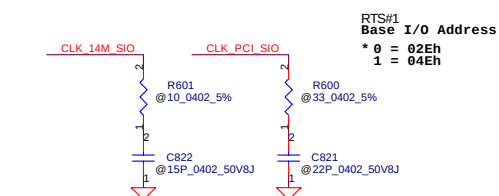
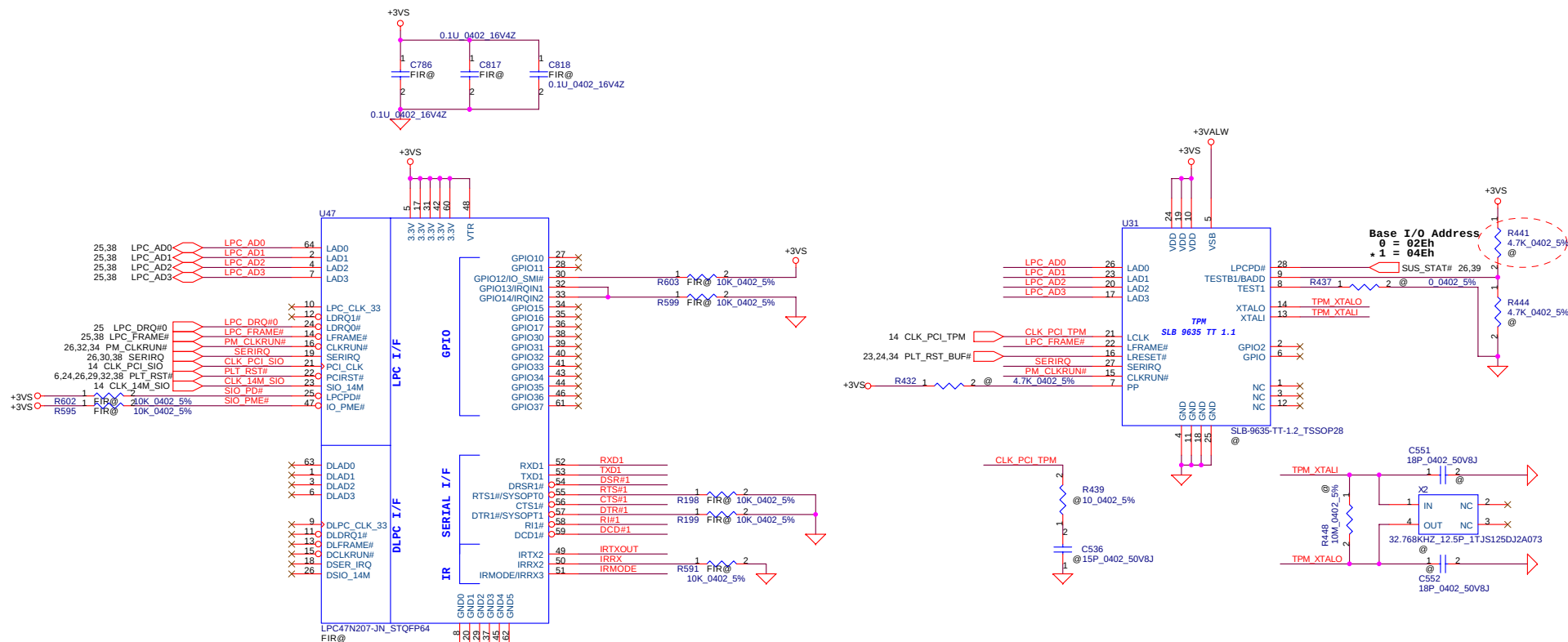
PHY PORT1

PCI I/F

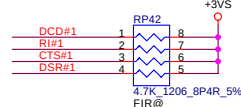
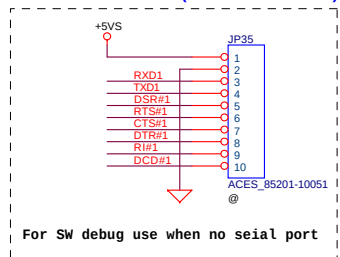
2005/12/18
Change P/N : SA00000P510

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								401454			
								Rev A			
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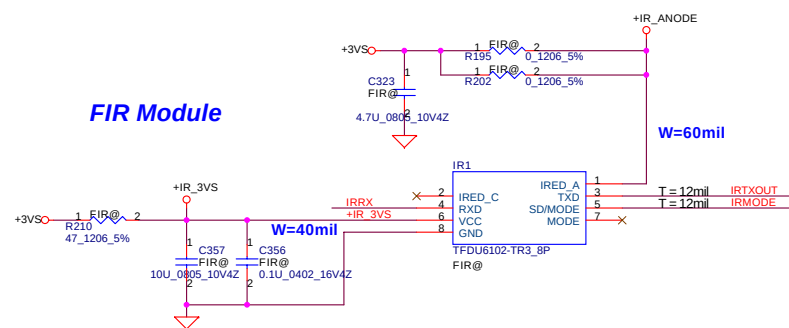
SUPER I/O SMsC LPC47N207



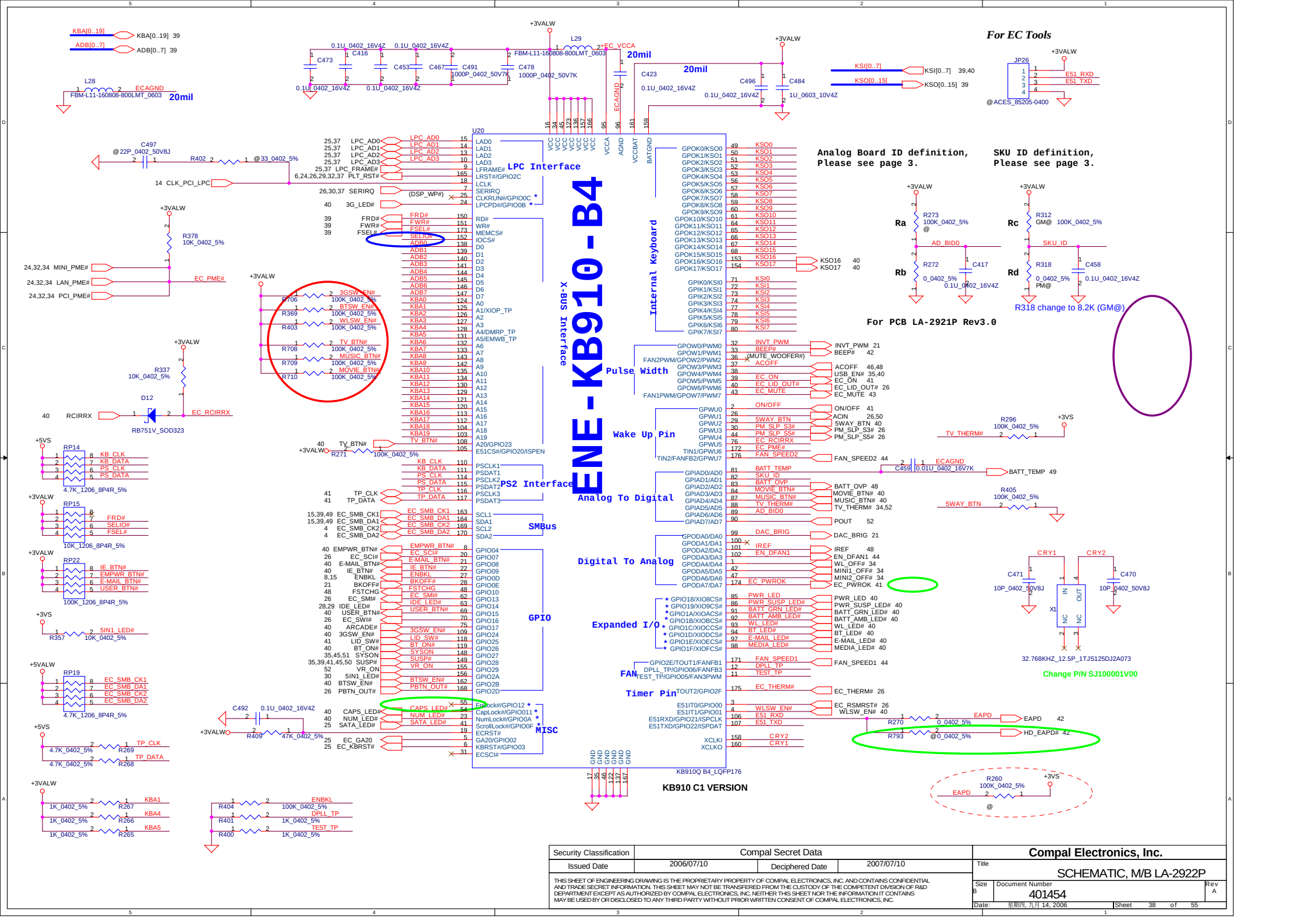
Place on the BOT side(near MINIPCI conn.)

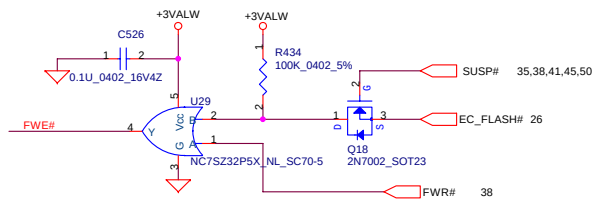


FIR Module

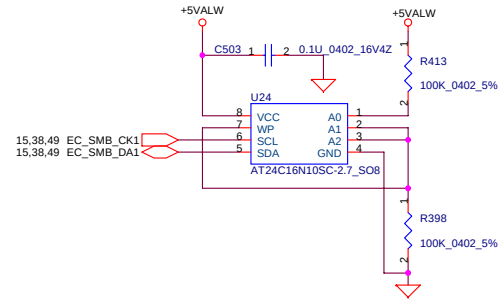


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				401454			
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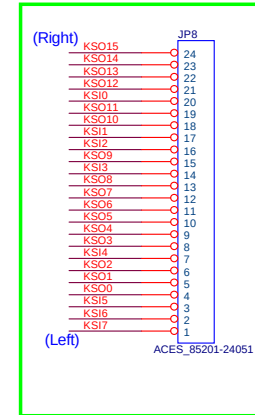
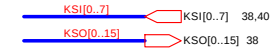




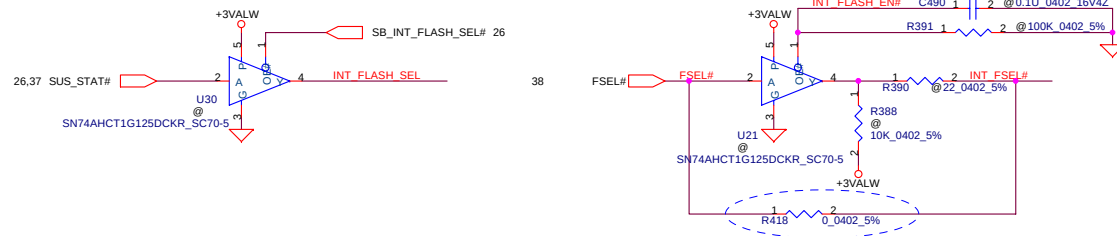
Check PCB Footprint



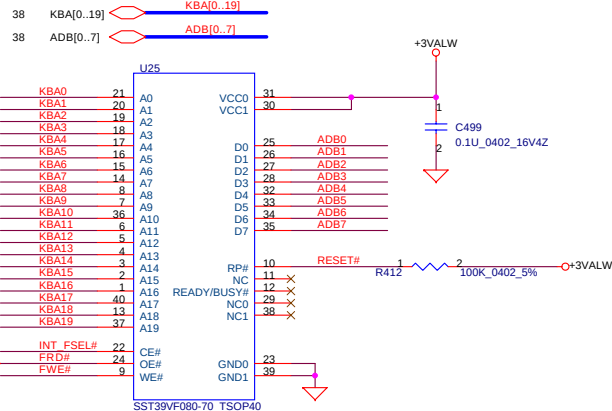
INT_KBD Conn.



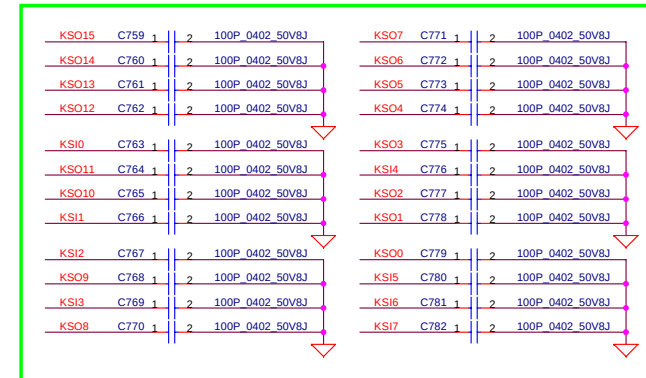
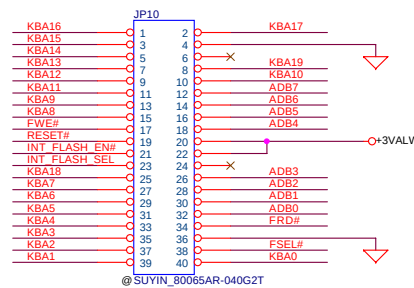
FOR DEBUG ONLY



1MB Flash ROM

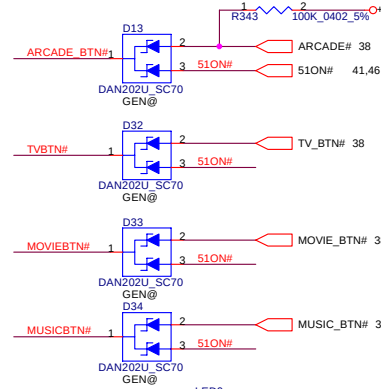
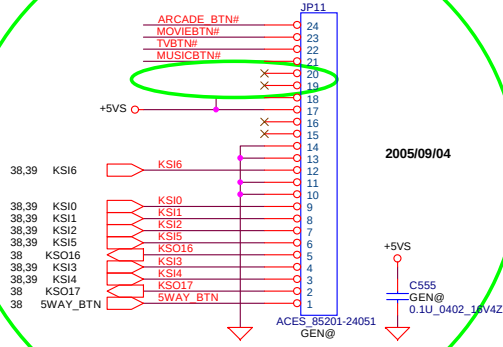


1MB ROM Socket

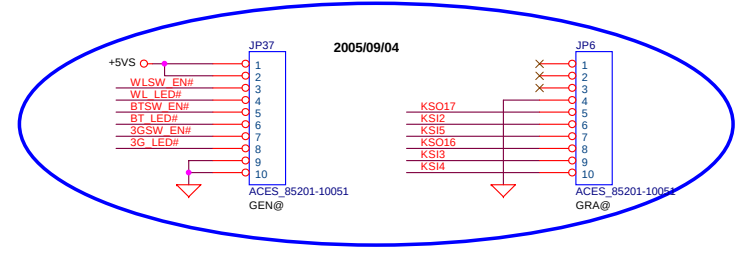
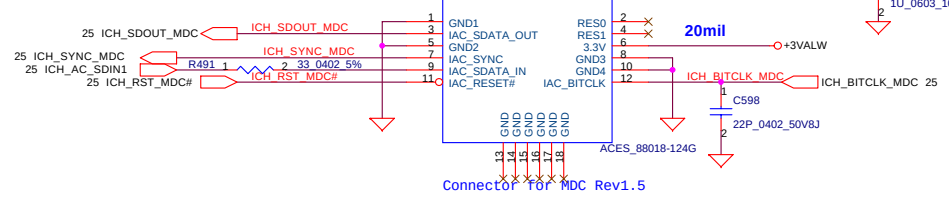


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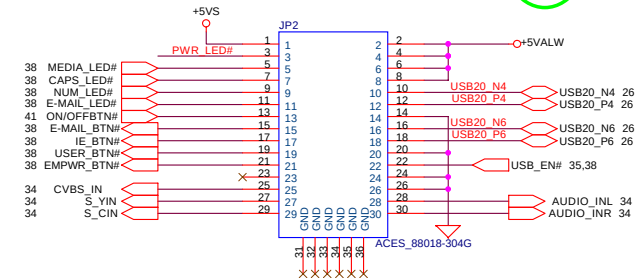
To CD-PLAY/B Conn.



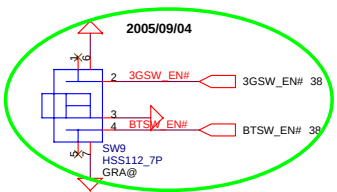
MDC Conn.



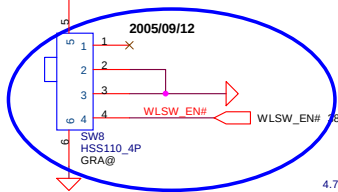
To LED/B Conn.



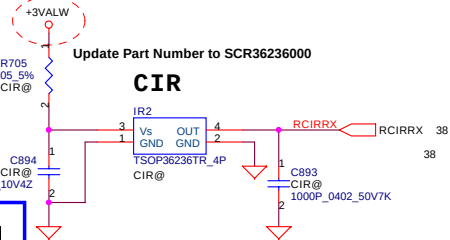
BT_SW & 3G_SW



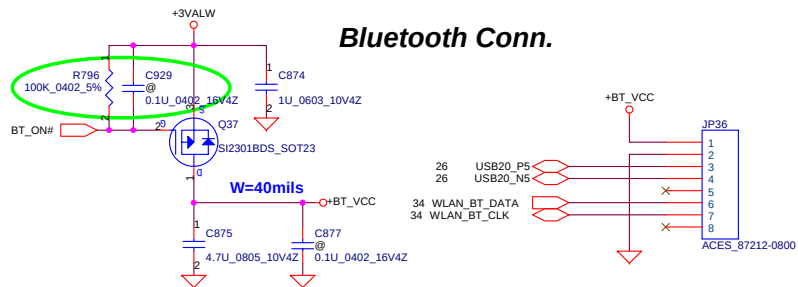
WL_SW



Geneva			Grapevine		
	KSO16	KSO17		KSO16	KSO17
KSI0	VOL_UP	LEFT			
KSI1	RIGHT	VOL_DOWN			
KSI2	PLAY	ENTER			
KSI3	STOP				
KSI4	NEXT				
KSI5	REV				
KSI6		RECORD			

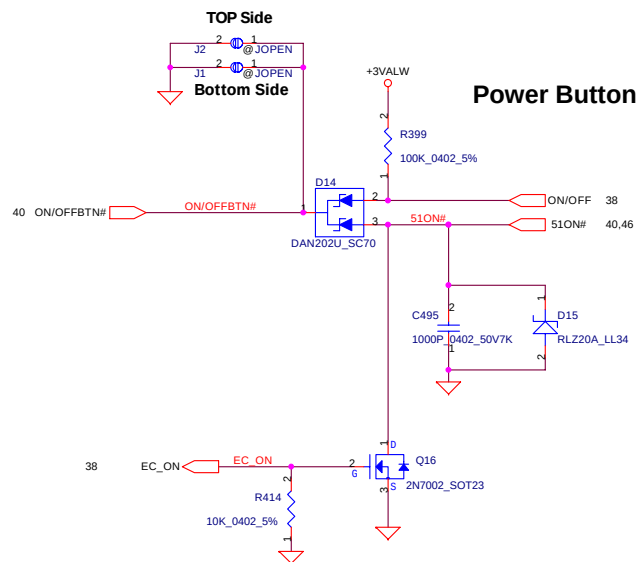


Bluetooth Conn.

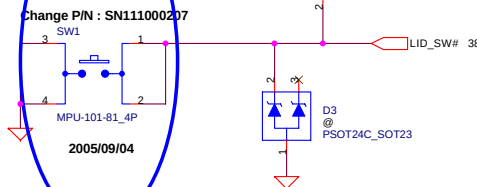


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ON/OFF switch

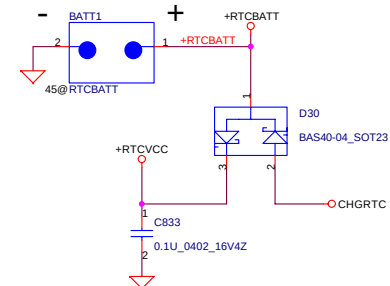


Lid Switch

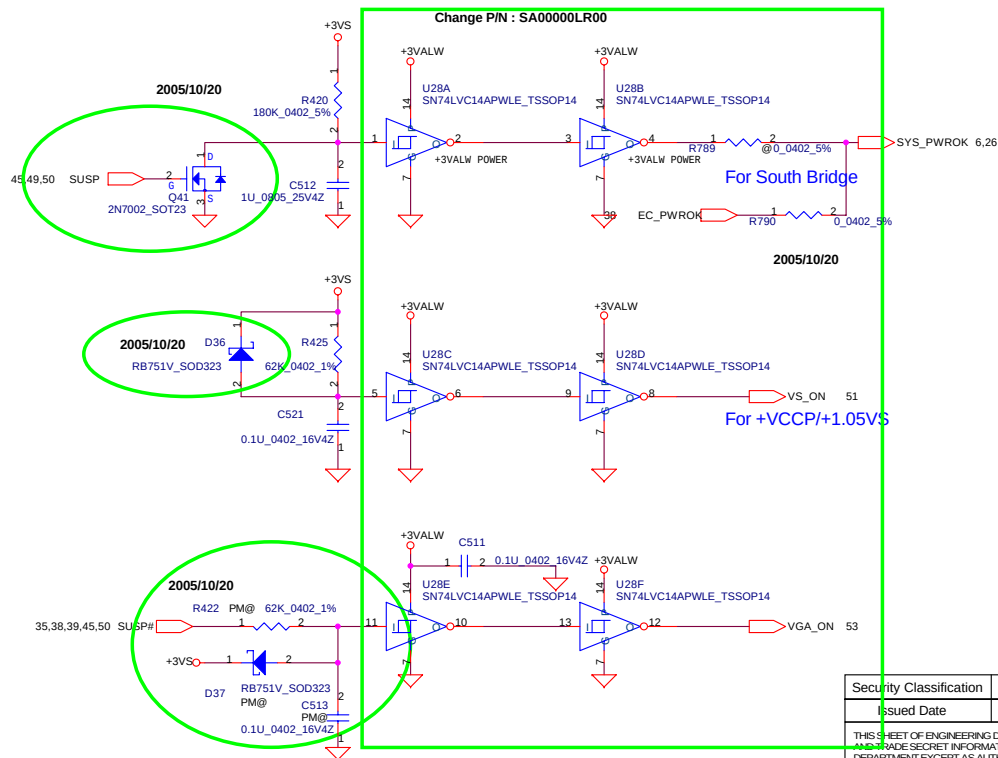


Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

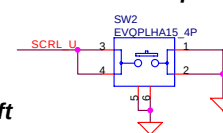
RTC Battery



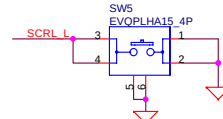
Power ON Circuit



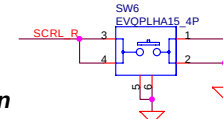
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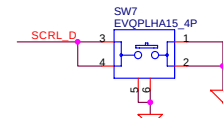
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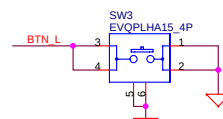
Scroll Right



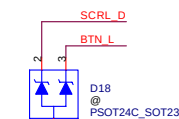
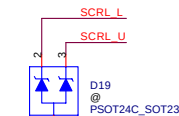
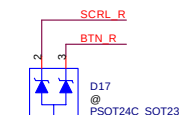
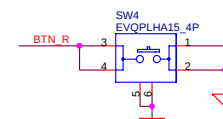
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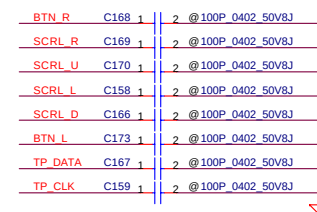
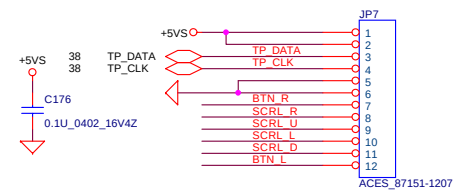
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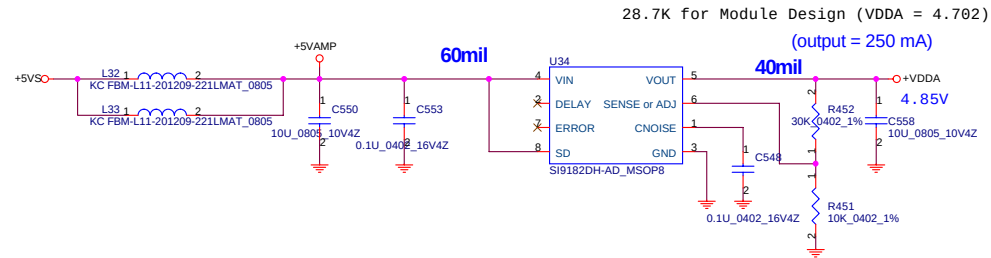
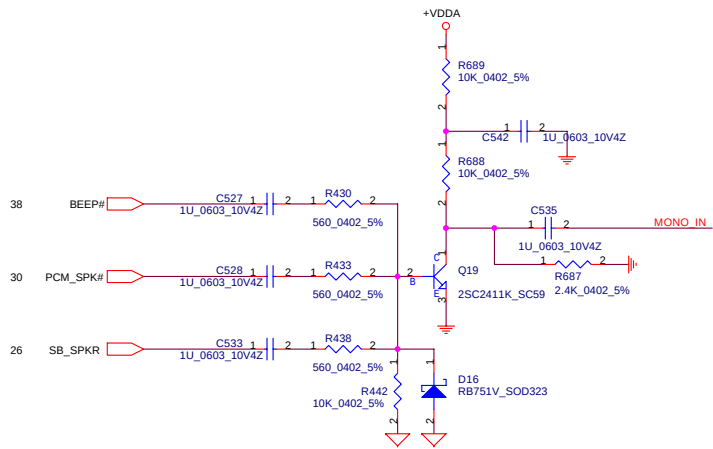
Right



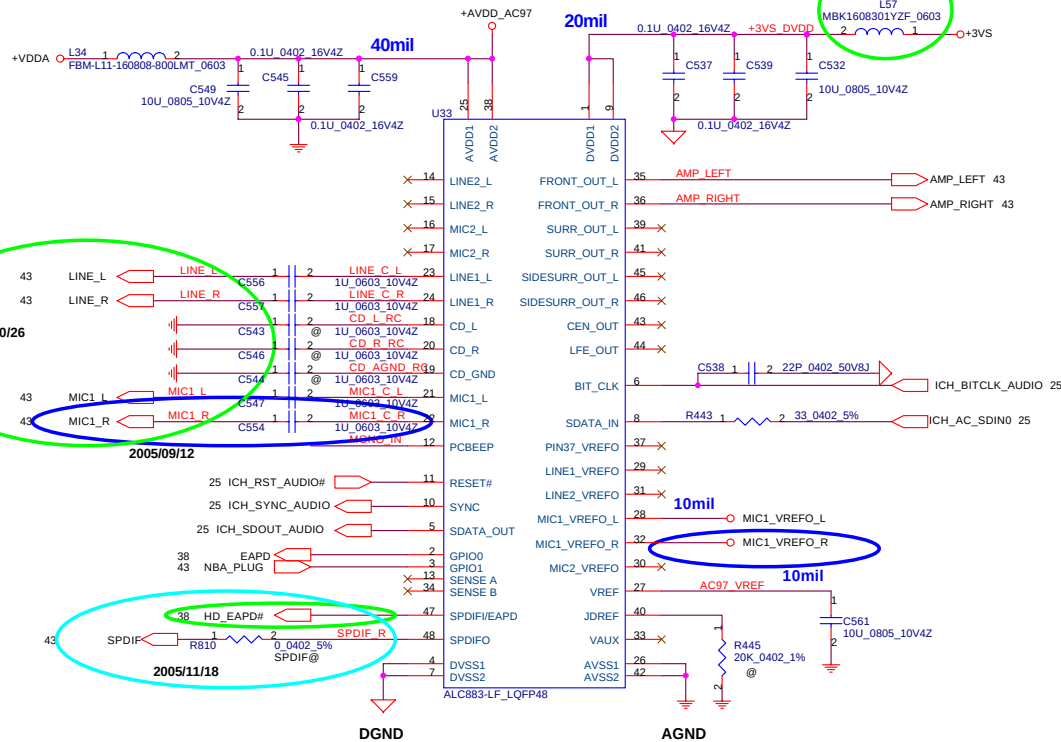
To TP/B Conn.



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HD Audio Codec

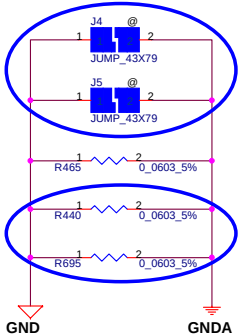


2005/10/26

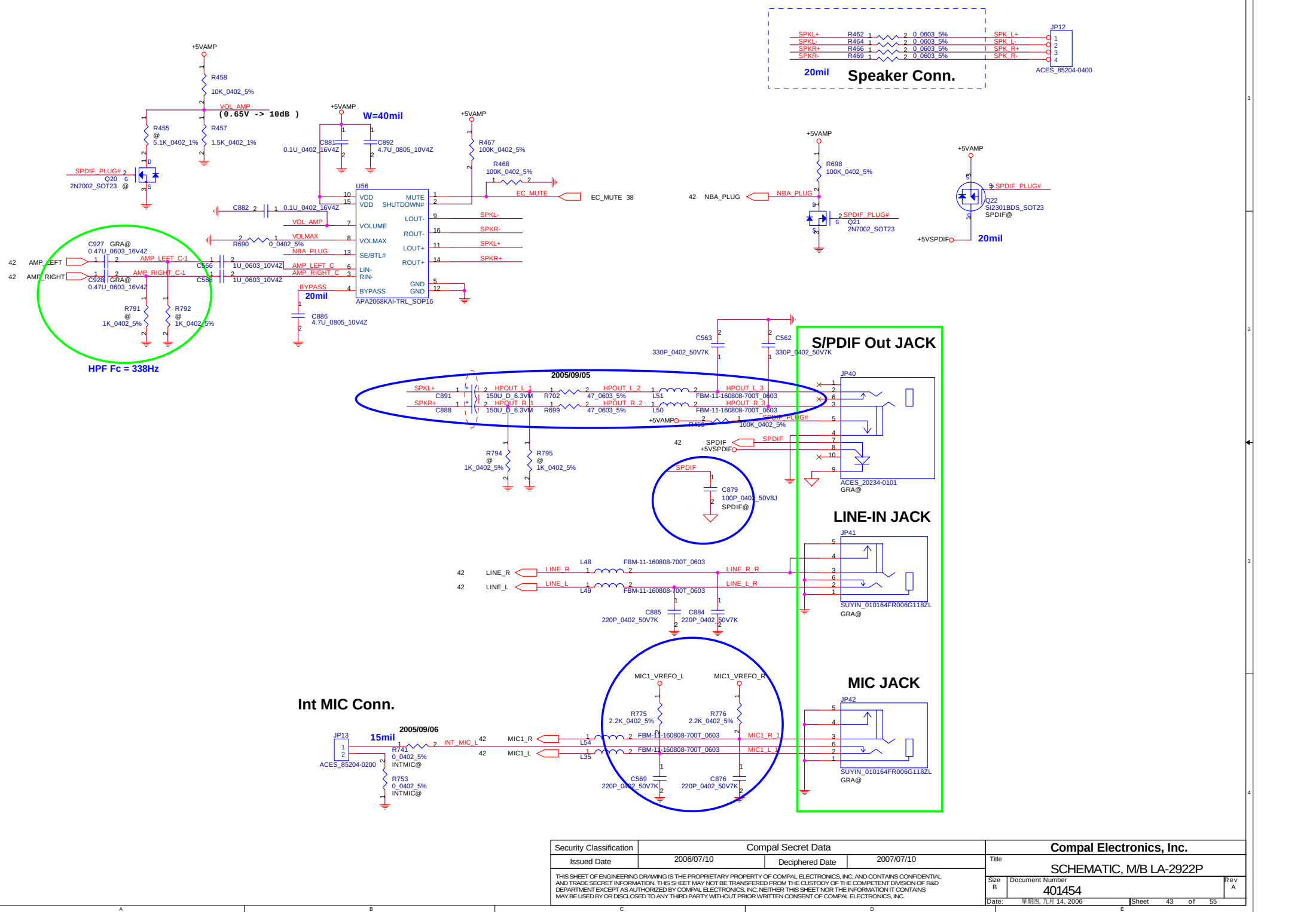
2005/09/12

2005/11/18

2005/09/20

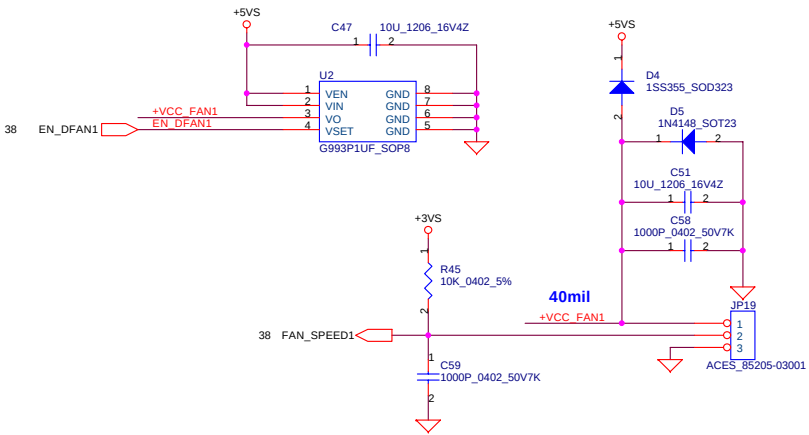


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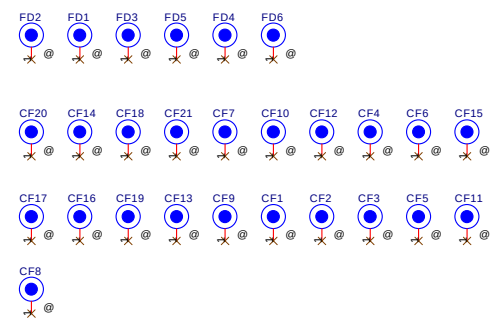
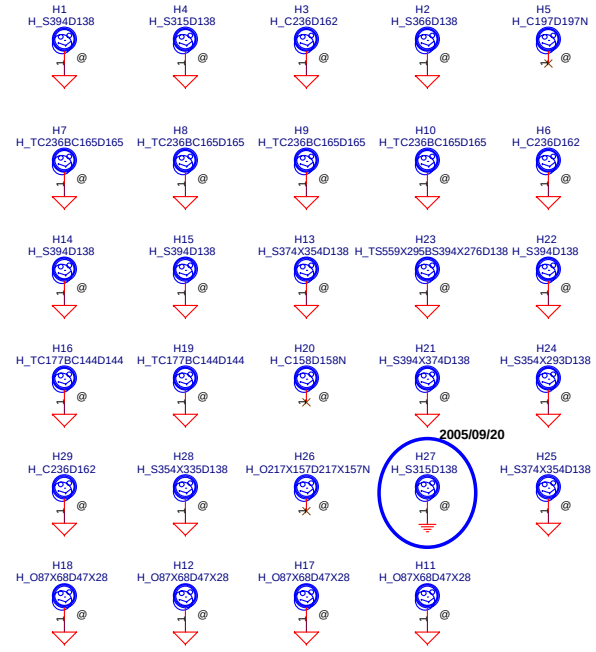
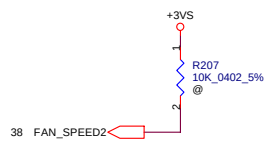


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FAN1 Conn

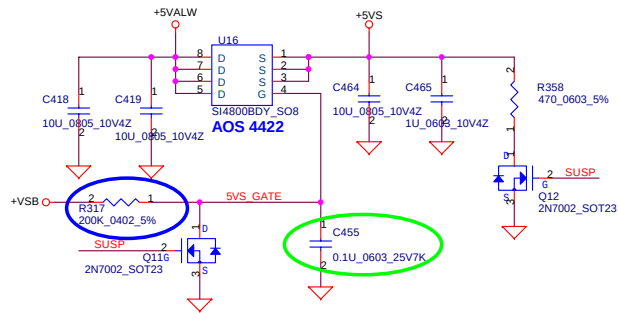


FAN2 Conn
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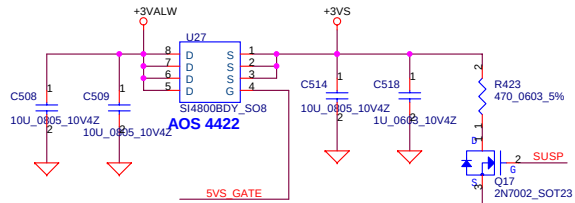


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+5VALW TO +5VS

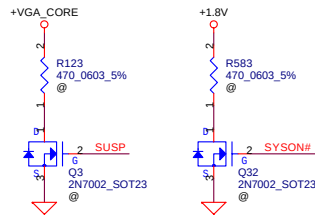
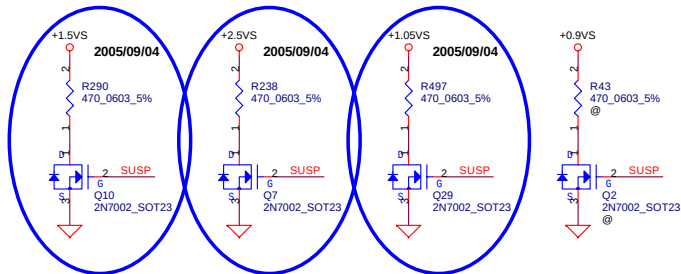
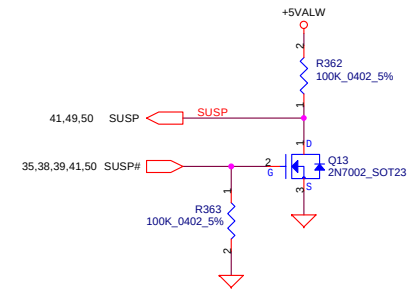
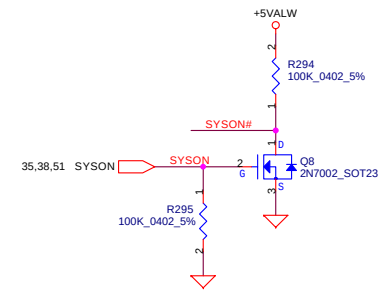
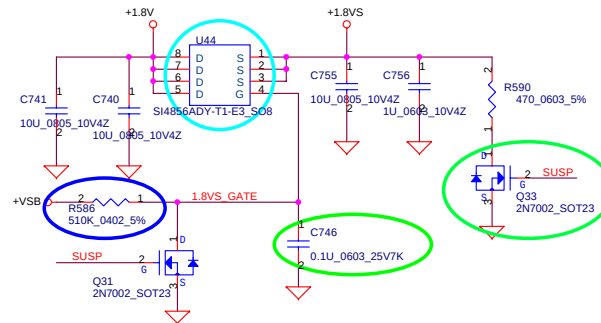


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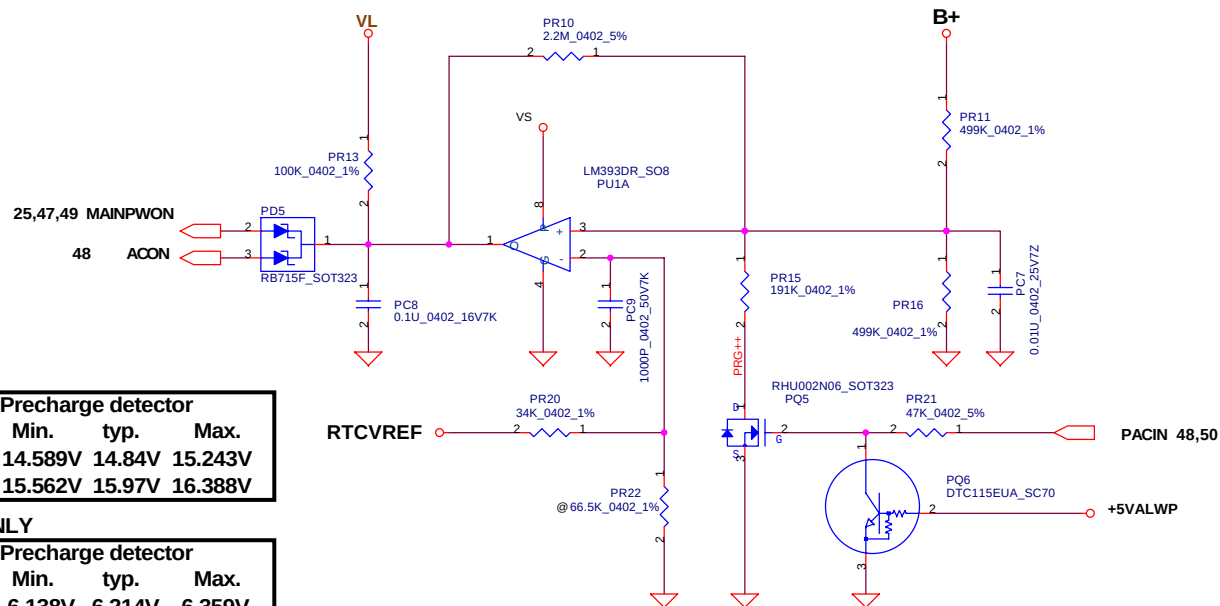
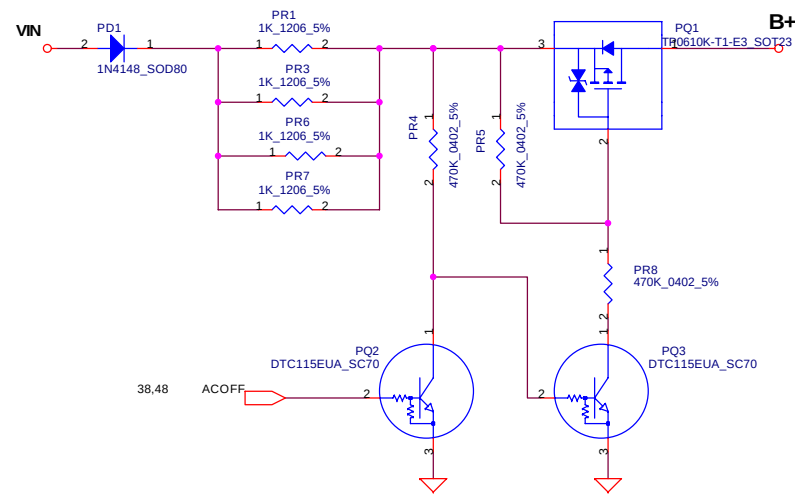


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SB54800310(Old)

+1.8V to +1.8VS

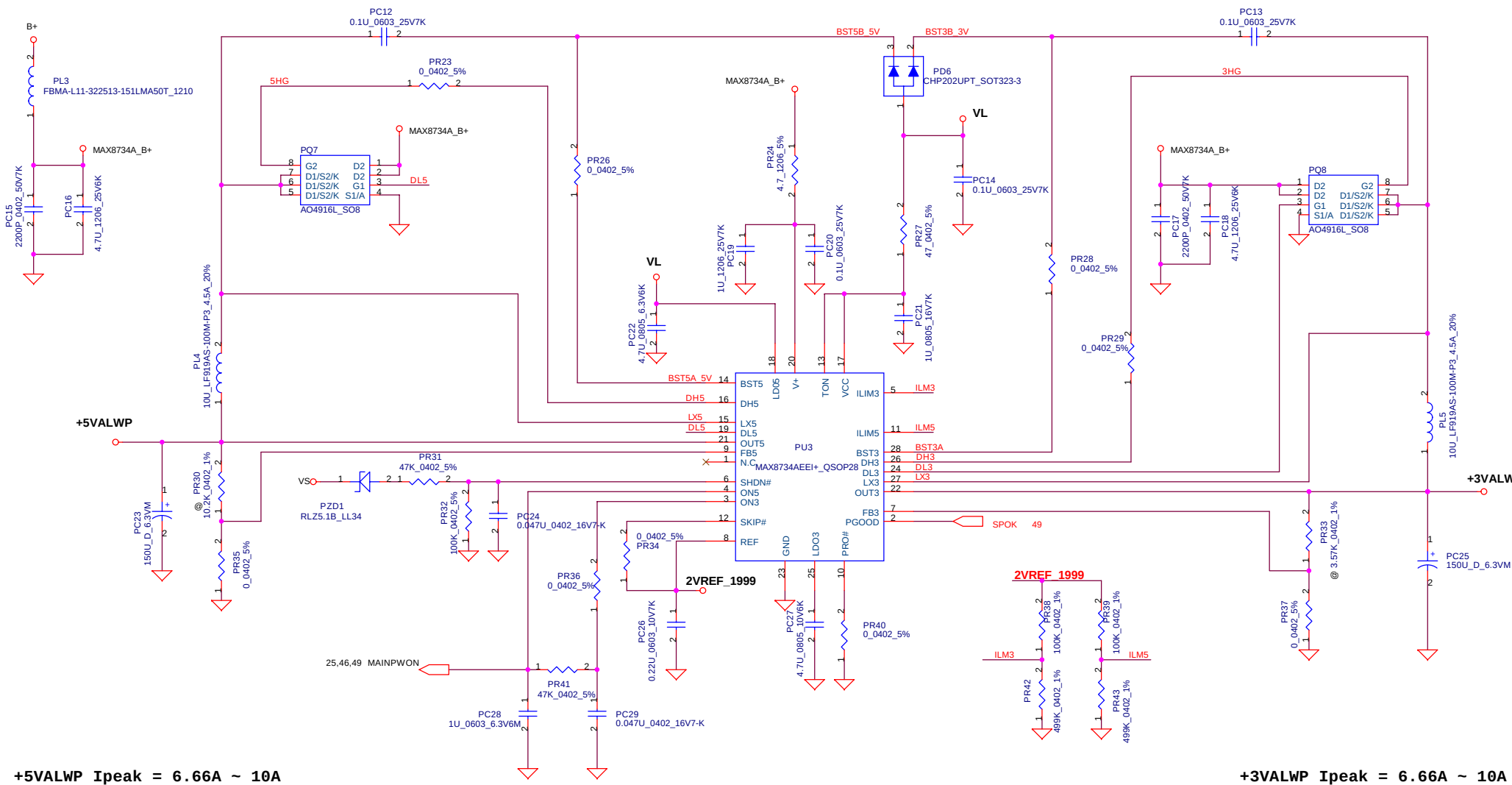


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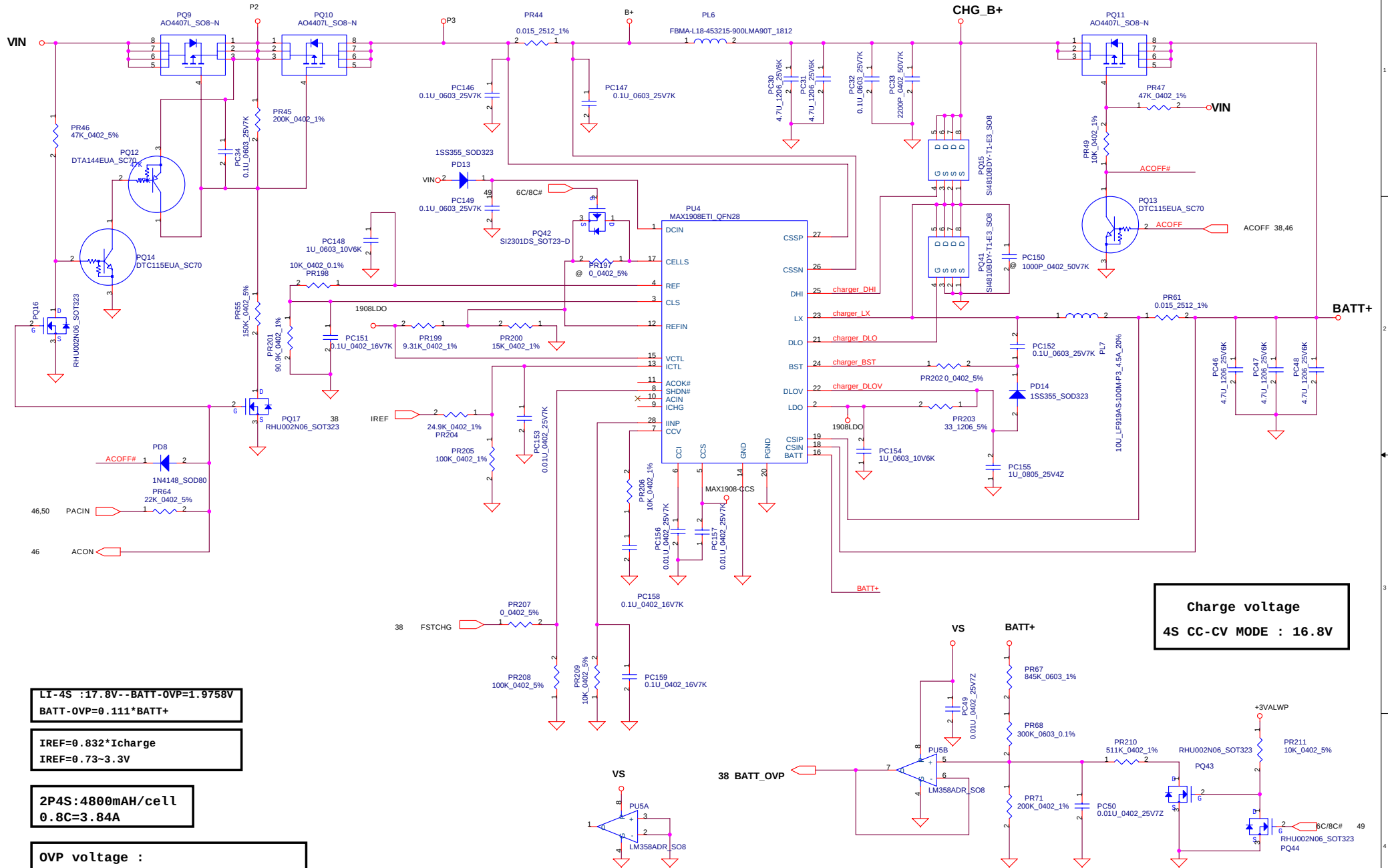
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H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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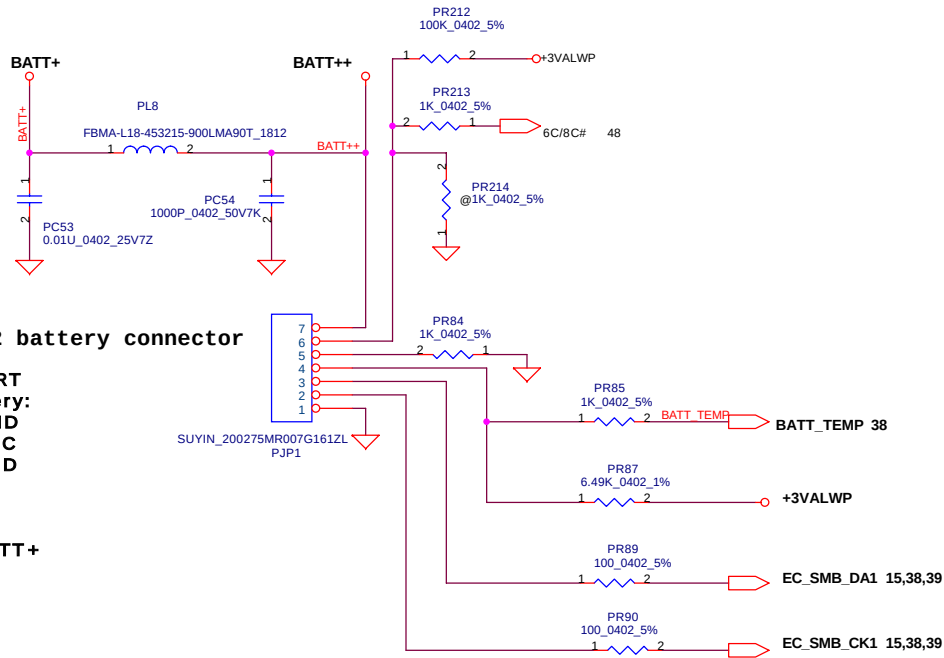
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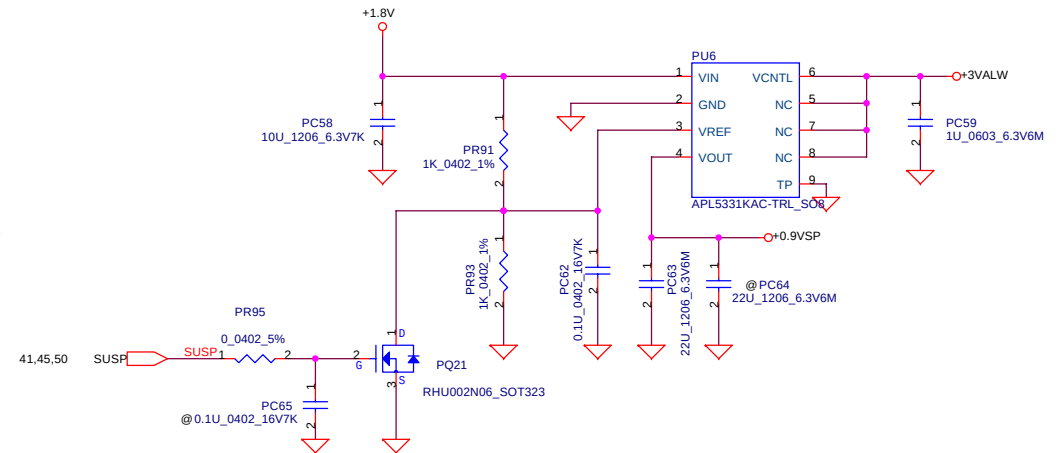
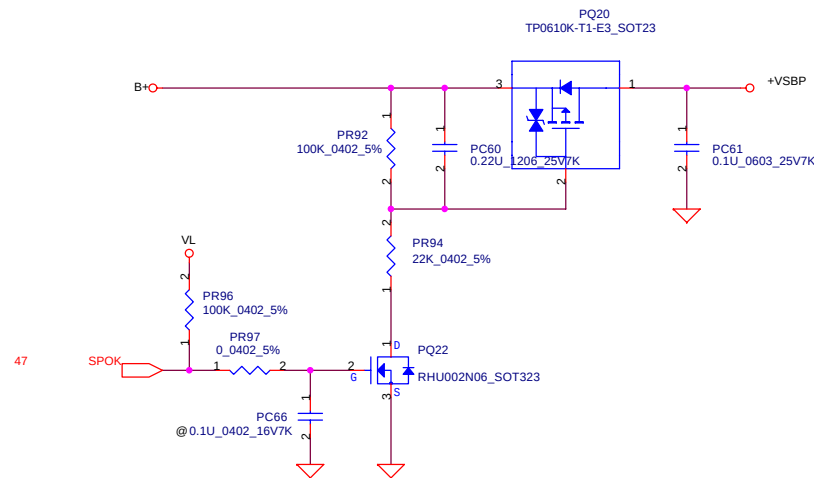
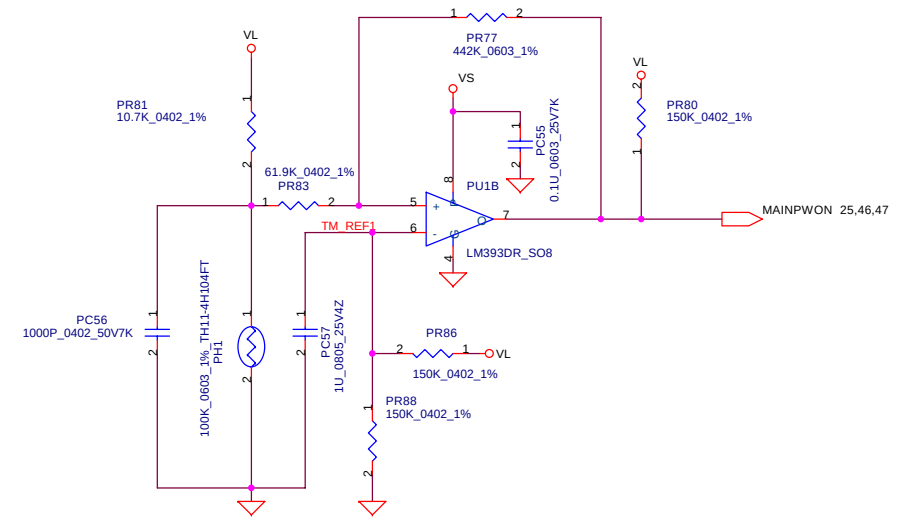
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PJP2 battery connector

SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+

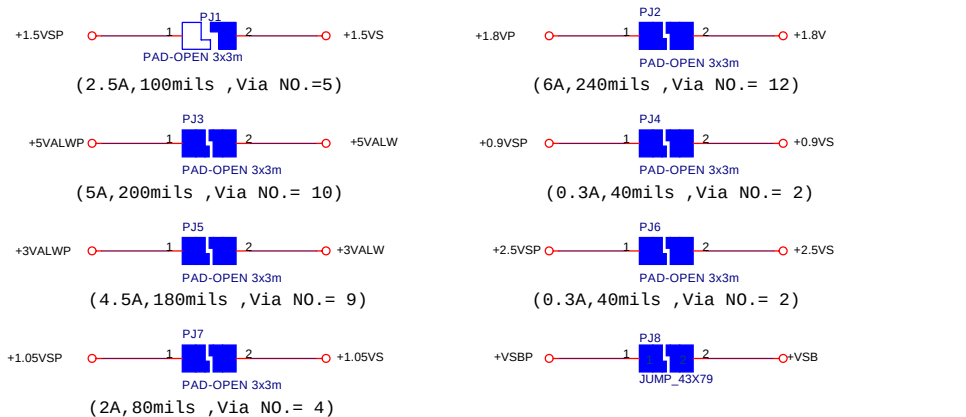


PH1 under CPU botten side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C

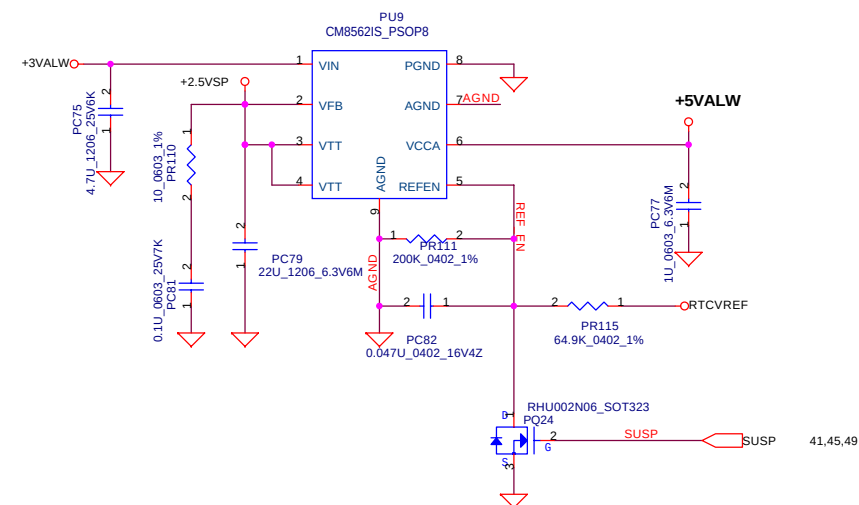
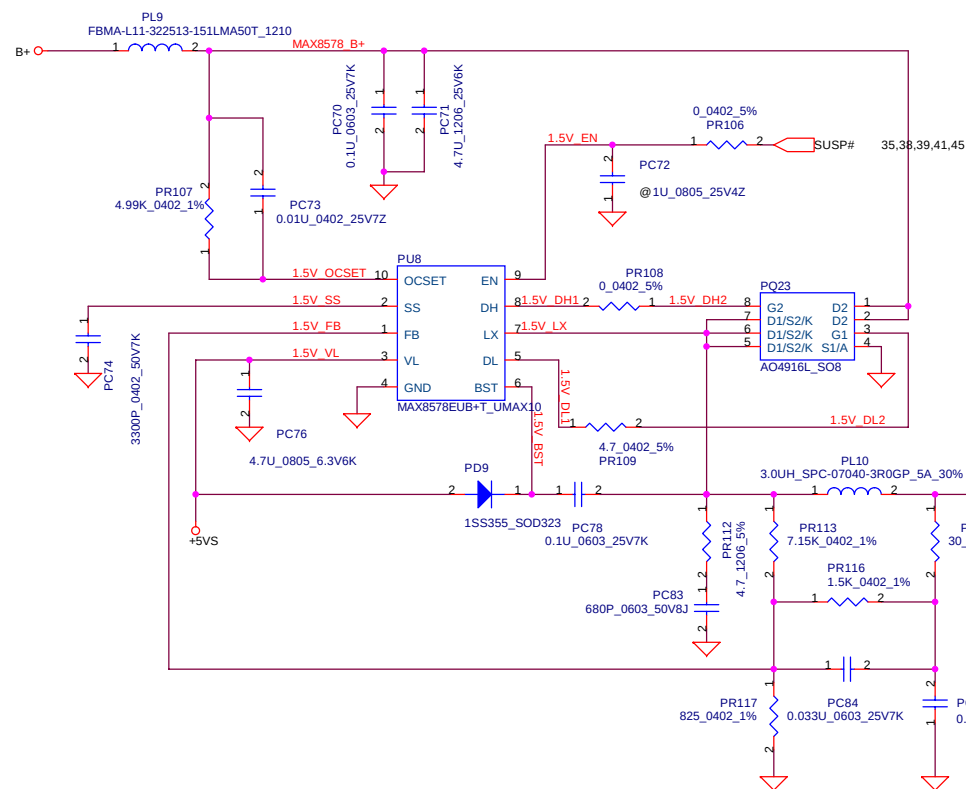
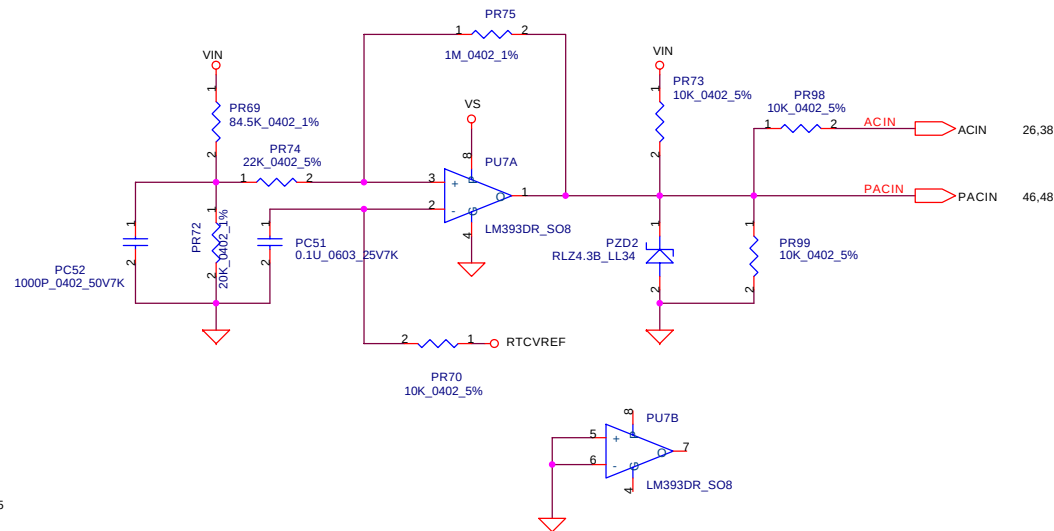


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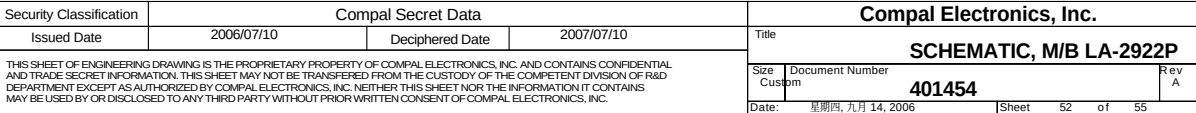
AC Adapter Detector



Vin Detector 17.90V/17.24V



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Rev 0.1 --> Rev 1.0 Change List

- 1. Page15 : Change BOM structure of R831 to VGA@
- 2. Page17 : Add C1110 to C1120 on power plane for EMI Require.
- 3. Page26 : Add BOM structure @ on D38 & R887

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